White Paper WP12

Ethernet ESD/Surge Compliance with AS1602

Revision 1.3
November 2007

Preliminary Information subjected to future revision and changes

System Analysis

Transient events can be either differential-mode or common-mode in nature. It's useful to understand the difference between the two types of events as the DUT components behaves differently under these type of events. A transient event is called a differential strike if the discharge can occur only through one of the 8-pins of the RJ45 connector. That is, the strike creates differential energy that can be transmitted across the Ethernet transformer (by definition, transformer couples differential energy across from RJ45 to the Ethernet Phy and vice-versa) to the Phy. This can occur in tests like IEC61000-4-2 (Air discharge) when discharge can occur through any one pin of the RJ45. Even a CDE or Cable Disconnect event can look like a differential event since mechanically not all RJ45 pins will make simultaneous contact.

A transient event is called a common-mode strike event if it is emulated with a cable plugged into the RJ45 connector and has capacitive coupling of the transient event evenly to the Ethernet cable through a capacitive clamp style device, as defined in EFTB standards like IEC61000-4-4. In this scenario each Ethernet signal pair sees the same transient behavior and the common-mode energy is blocked by the Ethernet transformer's isolation barrier.

To recap, a differential-mode transient strike will couple more transient energy to the Ethernet Phy as it passes through the Ethernet transformer, and is the major cause of damage to the Ethernet Phy. A common-mode strike couples less energy to the Phy; in most systems, common-mode survivability is limited by the 2kV isolation of the Ethernet transformer.

We can analyze the effect of a differential surge strike using the figure below. When a surge strike is done to any one RJ45 pin at a time, the currents are high enough to rapidly saturate the transformer core. However, even after saturation, there is some air-core based mutual inductance between the primary and secondary sides which will couple the energy along with inter-winding capacitance of the Ethernet transformer (typically 10-15pF). The Phy I/O protection circuit will shunt (via device snapback or body diode forward biasing) the residual surge energy to power/ground plane, providing a path back to earth ground (lowest impedance path either through power transformers as shown in the figure below or though other ports in the system like USB, RS232 ports etc, whichever presents lowest impedance path). The Bon-Smith termination resistor and capacitor shown on the line side center-tap also provides a path to earth ground and prevents build-up of large voltage across the transformer.

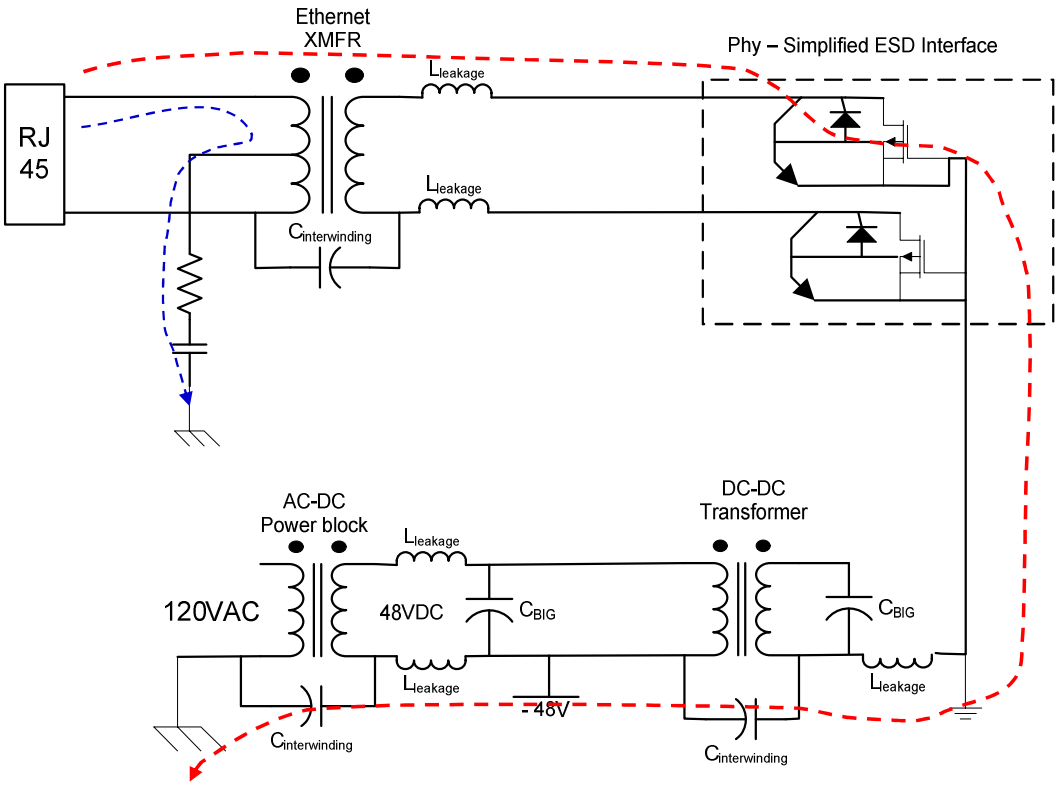

Figure 2: Schematic view of Surge relevant system components and Surge energy paths

Akros Silicon has created a detail simulation/analysis model of the components involved in the system and has further validated this model with measurements. The Ethernet interface illustrated here is the PHY, which is typically an open drain NMOS devices. When the voltage reaches a critical level, the NMOS device will snapback- which is illustrated in the diagram as a parallel bipolar device. This snapback device is not a well controlled device, but rather a parasitic device with strong process dependence. This device will fail if there is enough current pushed through it for a sustained duration.

Because of core saturation of the transformer, the surge energy transferred to the PHY is limited to the inter-winding capacitance of the transformer. For example, in IEC61000-4-2 the energy storage capacitor (as described in the earlier section) is 150pF and is charged up to 15kV (Level4) for a total charge of 2.25μC. The typical inter-winding capacitance range is from 5-15pF. During the strike, this charge is shared between the striking capacitor and the interwinding capacitor, and hence only 5-10% of surge energy goes through to the Phy side. The leakage inductance of the transformer helps slow down the transient waveform, however transferred surge energy is generally sufficient to cause destructive damage to many of the smaller-geometry Phys.

In a POE system, there are additional paths to the earth ground via POE-PD interface back via the AC-power block. However a similar analysis of surge energy transfer to Phy can be done for a POE system also.

AS1602 ESD Design and Usage

The AS1602 is designed to be placed between the Ethernet transformer and the Ethernet Phy for providing both ESD protection and CM/EMI Suppression on the differential data lines.

The AS1602 includes highly robust ESD/Surge protection circuits and programmable common-mode noise suppression circuits. At the system level, the AS1602 provides the Ethernet Phy with protection from ±25kV of IEC61000-4-2 air discharge strikes and ±12kV of Cable Discharge Events. The AS1602 is designed to provide at least 10dB of additional common-mode rejection (in addition to transformers rejection) to facilitate easy compliance to EMI emissions (CISPR22/FCC part15, class B) and immunity standards (IEC61000-4-3/4-6, Level3).

The AS1602 uses an open-drain output stage similar to that used in most Ethernet Phys, and the output is biased from the transformer center tap supply (VCT). This allows the AS1602 to work with all standard Ethernet transformers and Phys, and can be used in both Fast Ethernet (10/100Base-T) and Gigabit Ethernet (10/100/1000Base-T) systems. The AS1602 uses a small form factor QSOP16 package with flow-through routing capability so that the AS1602 can be placed right next to the transformer without use of any vias/stubs. This facilitates a very low inductance connection between the transformer and AS1602 that is critical for ESD performance.

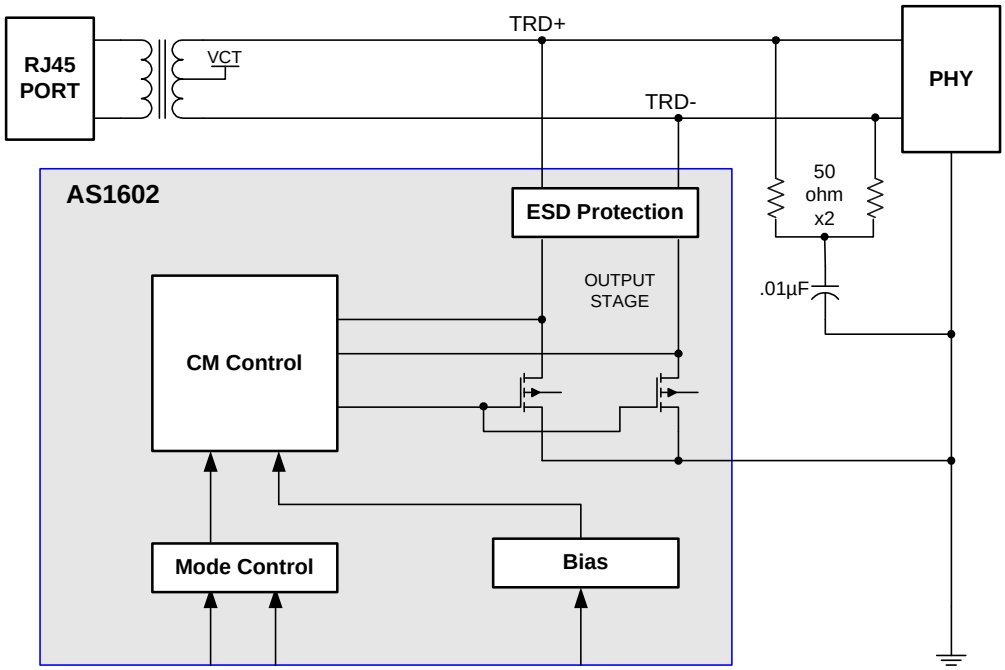

Figure 3: AS1602 block diagram and system schematic

Figure 4 below conceptually shows the output ESD structure of the AS1602 device. The AS1602 utilizes Akros' *proprietary* design hardening and layout techniques to achieve a very low inductive effect and low capacitive loading in the output ESD structures that is crucial in enabling robust ESD performance without impacting Ethernet electrical signal integrity.

Positive ESD strikes are handled through a stack of diodes that are biased to ensure operation using a wide range of Vdd and Vct supply voltages. Negative ESD strikes are handled through output NMOS bulk diodes, which are also hardened to handle large surge energy. The AS1602 design prevents snapback of the PHY output NMOS devices by fast turn-on and efficient energy dissipation through ESD structures. Proprietary design techniques allow the design to handle both moderate energy/fast transients that create high thermal stress as well as high energy/slow transient events that create tremendous voltage overstress.

As shown in the figure 4 below, the AS1602 reference design utilizes small ferrite beads between the AS1602 and the Ethernet Phy (see AN060 – AS1602 Design Guide for details). These ferrite beads help direct surge energy through the AS1602's robust ESD structures and prevent any surge energy through the Ethernet Phy. This prevents the Phy from seeing any significant overvoltage stress and can enable system designers to use very small geometry Phys that have limited direct ESD capabilities.

Since the AS1602 is working between each signal node and the power/ground plane, it's capable of handling both differential ESD strikes and common-mode ESD strikes, enabling system designers to utilize it for meeting all ESD compliance needs.

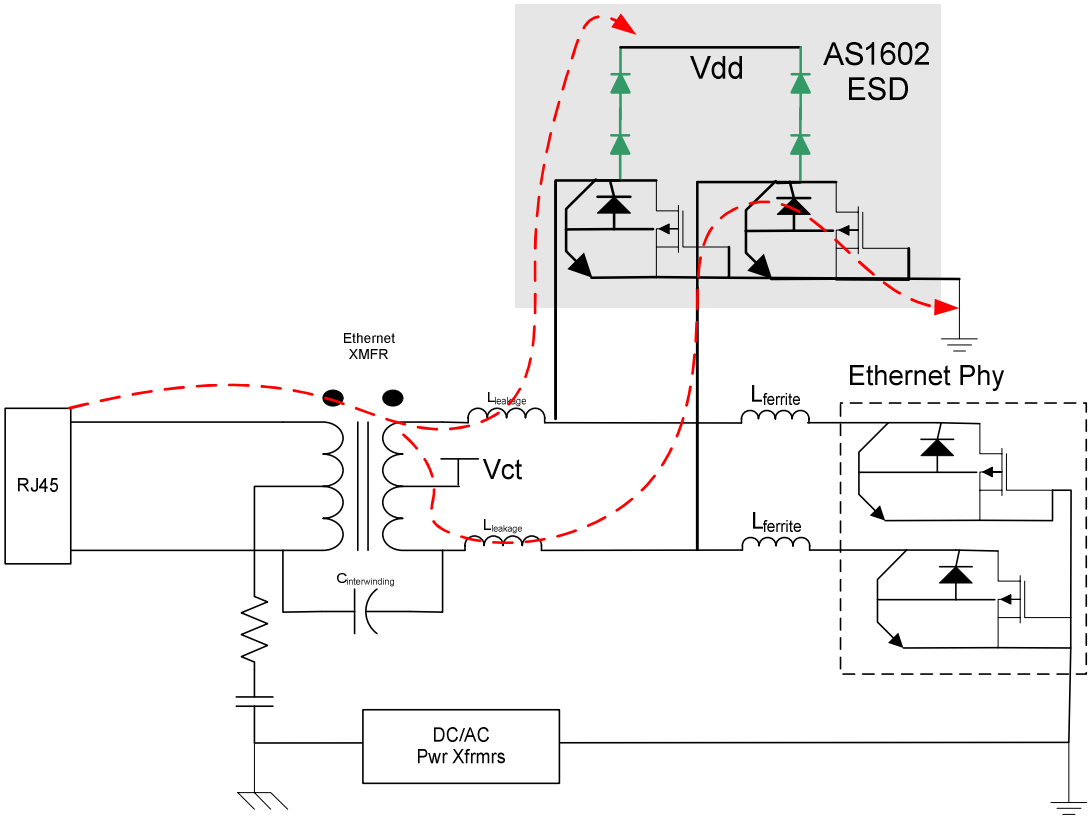

Figure 4: AS1602 ESD structure and strike path analysis

ESD/Surge Test Results

Akros has tested ESD/Surge performance of the AS1602 at both a system level and as a standalone device. Testing was performed using a popular Gigabit Ethernet Phy on an Ethernet evaluation board with a recommended Ethernet transformer. System ESD testing was done on these boards both with and without the AS1602 to establish effect of the AS1602 on ESD performance. This testing done internally and validated by an external independent EMC Compliance lab as would be necessary for system level product qualification.

Below table summarizes the test results from the external compliance lab testing. The testing was done in 1kV increments. EUT GbE functional reach testing (120m CAT5) is done to establish pass/fail threshold, along with other parametric measures.

Table 1: Compliance Lab Test Results

Test	Phy Only w/ Transformer	Phy w/ AS1602 w/ Transformer	Improvement by AS1602
Air Discharge IEC61000-4-2	Pass ±11kV	Pass ±29kV	**18kV**
Cable Discharge Equivalent	Pass ±8kV	Pass ±15kV	**7kV**

Compliance testing report from independent lab is available from Akros upon request.

As shown in table 1, the AS1602 is a very robust ESD/Surge protection device for Ethernet equipment, far exceeding performance of standalone PHYs. In above testing, the AS1602 exceeded its own target datasheet specifications of ±25kV for Air-Discharge and ±12kV for CDE in Ethernet systems.

AS1602 – A unique solution for Ethernet port EMC Compliance

The AS1602 is designed to address Ethernet port EMC compliance issues routinely faced by system designers. EMC compliance is one of the most challenging issues system designers must resolve, often times requiring extensive debug efforts, multiple board spins, and resulting in product cost increases and platform launch delays. The AS1602 is designed to reduce that overhead and ease system design for EMC compliance, enabling rapid product development cycles and reuse of robust designs.

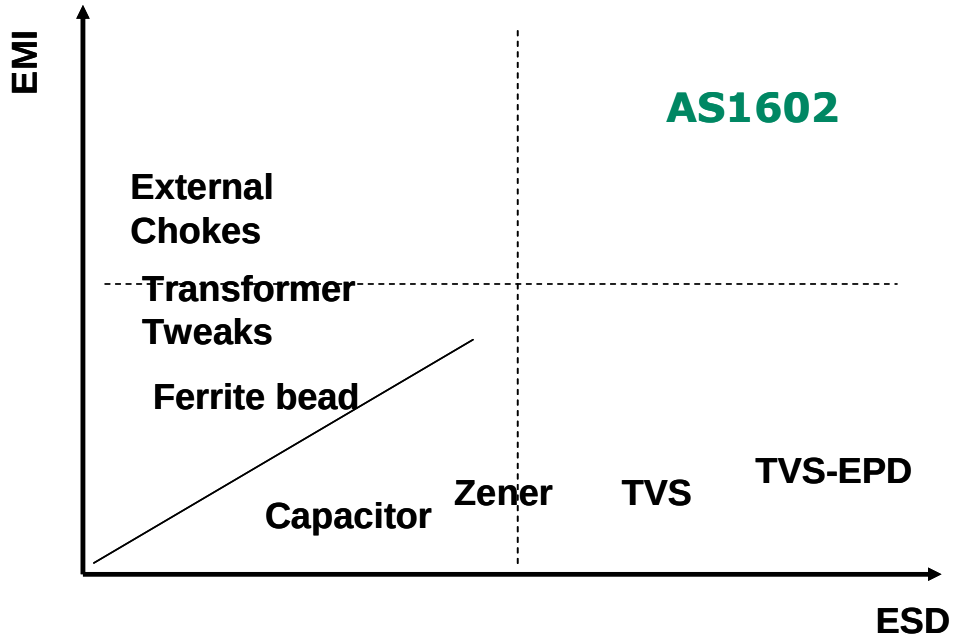

Figure 5: AS1602 positioning and comparison with other available products

The above figure shows a comparison and the positioning of the AS1602 compared to other choices/products available in the market place. AS1602's combination of Active EMI suppression and ESD Protection in one small package is a compelling solution for Ethernet system designers with EMC compliance challenges. The AS1602s ease of design, limited board space requirements, and ability to improve time to market product introductions dramatically improves issues associated with EMC compliance.

References

AS1602 Advance Datasheet, Akros Silicon

AN060: AS160X Design Guide, Akros Silicon

WP11 – EMI Compliant 802.3af PD Design with AS160X & AS1100

AS1602 External ESD Compliance Report – AS1602_ESD-(EN-IEC61000-4-2)_030848, HP Roseville Hardware Test Center

Contact Information & Notices

Headquarters
Akros Silicon Inc.
6399 San Ignacio Ave, Suite 250, San Jose, CA 95119
USA
Tel: (408) 746-9000 ext. 100
Fax: (916) 351-8102
Email inquiries:
marcom@akrossilicon.com
Website: www.akrossilicon.com

Regional Offices
Northern CA

Akros Silicon, Inc.
1296 Kifer Road, Suite 603
Sunnyvale, CA 94086
Tel: 408-746-9000

Canada

Brian Turner and Associates
51 Cecil Walden Ridge, Kanata
ON K2K 3C6 Canada
Tel: 613-254-9024
Website: www.btai.ca

Important Notices

Legal Notice

Akros Silicon™ assumes no responsibility or liability for information contained in this document. Akros reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or services without notice. The information contained herein is believed to be accurate and reliable at the time of printing.

LIFE SUPPORT POLICY

LIFE SUPPORT: AKROS' PRODUCTS ARE NOT DESIGNED, INTENDED, OR AUTHORIZED FOR USE AS COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS. NO WARRANTY, EXPRESS OR IMPLIED, IS MADE FOR THIS USE. AUTHORIZATION FOR SUCH USE SHALL NOT BE GIVEN BY AKROS, AND THE PRODUCTS SHALL NOT BE USED IN SUCH DEVICES OR SYSTEMS, EXCEPT UPON THE WRITTEN APPROVAL OF THE PRESIDENT OF AKROS FOLLOWING A DETERMINATION BY AKROS THAT SUCH USE IS FEASIBLE. SUCH APPROVAL MAY BE WITHHELD FOR ANY OR NO REASON.

"Life support devices or systems" are devices or systems which (1) are intended for surgical implant into the human body, (2) support or sustain human life, or (3) monitor critical bodily functions including, but not limited to, cardiac, respirator, and neurological functions, and whose failure to perform can be reasonably expected to result in a significant bodily injury to the user. A "critical component" is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

SUBSTANCE COMPLIANCE

With respect to any representation by Akros Silicon that its products are compliance with RoHS, Akros Silicon complies with the Restriction of the use of Hazardous Substances standard ("RoHS"), which is more formally known as Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. To the best of our knowledge the information is true and correct as of the date of the original publication of the information. Akros Silicon accepts no duty to update such statements