Application Note AN064

20W PoE Reference Design with Integrated Protection

- Meets EMC Class B Specification with >25kV ESD Protection
- AS1124 - AS1602 - BCM5481

Revision 0.5
Dec. 2007

Preliminary Information subjected to future revision and changes
REVISION HISTORY

The revision history of the AN064 reference design document is shown in Table 1.

Table 1 AN064 Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Author</th>
<th>History Details</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>D.Jolly</td>
<td>Initial release of AN064 document for review</td>
<td>09-04-07</td>
</tr>
<tr>
<td>0.2</td>
<td>J.Glick</td>
<td>Re-format AN064 document for review.</td>
<td>10-01-07</td>
</tr>
<tr>
<td>0.3</td>
<td>J.Glick</td>
<td>Update AS1602 information to document and release for review.</td>
<td>11-17-07</td>
</tr>
<tr>
<td>0.5</td>
<td>S. Gu</td>
<td>Update title and schematics</td>
<td>11-26-07</td>
</tr>
</tbody>
</table>

MANUAL ORGANIZATION

This document uses the following sections to provide DESIGN details:

- **Introduction** — Includes a block diagram and overview section.
- **Product Features** — Summary of product feature list for AS1124, AS1602 & BCM 5481.
- **Reference Design Implementation** — Includes a functional description of each of the interface blocks.
- **Reference Design Schematics**
- **Design Layout** — Includes considerations for layer assignments, signal trace design, and general circuit board layout.
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INTRODUCTION

The development of Power over Ethernet (PoE) technology has given rise to a number of applications that combine the use of the RJ45 connector as both a data port and power interface. Expanding the guidelines defined by the IEEE® 802.3af™ standard, the proposed IEEE 802.3at™ standard (PoE plus) answers demands for increased power requirements per port and flexibility for power management in such systems, especially those that support the emerging triple play media processing environment.

The AS1124-AS1602-BCM5481 reference design provides an example of such a system, implementing a Reduced Gigabit Media Independent Interface (RGMII) that provides data stream support and incorporating a power management system of 24W. The design employs devices to minimize signal noise that could corrupt transmitted data; to meet tougher EMI Emission (CISPR22 and FCC Part 15, Class B requirements) and/or EMI Immunity standards (IEC61000-4-3/6 requirements for Radiated and Conducted Immunity, Level 3 or higher); and to support an unprecedented level of protection by enabling the PoE application system to pass ± 25kV air discharge (IEC61000-4-2 specifications) and ±12kV CDE (Cable Discharge Event).

This document provides details about PoE reference design and is intended for engineers designing PoE devices using the powered device (PD) side of the network. This design includes implementation details, schematics and block diagrams. For simplicity, this document refers to the AS1124-AS1602-BCM5481 Reference Design as the DESIGN throughout.

OVERVIEW

The RJ45 supports Unshielded Twisted Pair (UTP) signals grouped as differential signals over CAT5 cable. The RJ45 interface provides Data (AC Signals) plus Power (DC Signals) for the DESIGN. The data rate supports 1GBE speeds and the power supports up to 24 Watts using 4 differential signal pairs.

The UTP signals contain DC plus AC signal components. The DC component provides the +48V for the PoE power requirements, whereas the AC component provides the 1GBE modulation signaling used for the XMT & RCV directions of the PHY.

The AS1602 provides circuitry for meeting tougher EMC Compliance (both EMI and ESD) in early phase of the system design and enables “Design for EMC” concept.

The DC is removed from the UTP cable using the 1GBE transformer center-taps. The 4 center-taps signals are routed directly to the AS1124 device, which performs the Powered Device DC Controller function. The output voltage levels from AS1124 device is +12V, which is used for power the entire design. The +12V can be converted into +3.3V or lower depending on the power supply requirements.

The AC component is passed directly to the 1GBE PHY (BCM5481), which processes the XMT & RCV 1GBE modulation signaling. The 1GBE PHY converts the analog differential signals into equivalent high speed digital signals using RGMII method of signaling between the PHY and MAC devices.

![AS1124-BCM5481 Block Diagram](image-url)
PRODUCT FEATURES

The DESIGN provides proven technology with low-cost components that support rapid development of PoE Ethernet applications to support emerging market requirements. It offers an optimal solution that balances clock frequency and pin count for the data transmission in the Ethernet interface and provides an efficient and low-cost solution for providing a regulated and low-EMI power system for PoE PDs with integrated surge protection for IEC61000-4 compliance. Because the devices do not require special thermal handling or heat-sinks, the DESIGN minimizes required board space and height. The DESIGN also represents a competitive advantage in reducing time-to-market in developing applications quickly.

REFERENCE DESIGN BLOCK DIAGRAM

Figure 2 AS1124-AS1602-BCM5481 Reference Design Block Diagram
BCM5481 Features

- Single-Chip integrated triple-speed Ethernet transceiver – MAC to Magnetics:
  - 1000Base-T IEEE Std. 802.3ab
  - 100Base-T IEEE Std. 802.3u
  - 10Base-T IEEE 802.3® standard
- GMII, RGMII and MII MAC interface options.
- Ethernet @ WireSpeed™
- Integrated voltage regulators
- Trace matched output impedance
- Lineside loopback
- Low electromagnetic interference (EMI) emissions
- Cable plant diagnostics
- Robust cable sourced electrostatic discharged (CESD) tolerance
- Support for jumbo packets up to 10 KB
- Detection and correction of pair swaps (MDI crossover), pair skew, and pair polarity
- Advanced power management
- IEEE Std. 1149.1™ (JTAG) boundary scan
- Super isolate mode
- 9 x 9 mm, 100-pin FBGA Package

AS1602 Features

- Enables system designers to comply with:
  - CISPR22 and FCC Part 15, Class B requirements for Radiated and Conducted Emissions.
  - IEC 61000-4-3/6 requirements for Radiated and Conducted Immunity.
  - IEC 61000-4-2 (Air Discharge) of ±25kV.
  - Cable Discharge Event (CDE) of ±12kV.
- Provides up to 10dB of additional common-mode noise suppression over a frequency of 1MHz to 125MHz when used with Ethernet magnetics.
- Robust built-in ESD protection provides additional protection for PHY and improves system ESD performance.
- JESD22-A114, ESD, HBM of ±8kV
- Interfaces to standard Ethernet transformers and 10/100/1000 Ethernet PHYs.
- Uses a single standard power rail (3.3V or 2.5V).
- Open drain output stage that can be biased from 1.8V to 3.3V using transformer center-tap supply as needed based on choice of Ethernet PHY.
- Flow-through routing for ease of board layout.
- Typical power consumption of 90mW.
- Low power mode available for tight power budgets.
- Industrial temperature range (-40°C to 85°C).
- Package size QSOP-16PINs.

AS1124 Features

- Fully supports IEEE Std. 802.3af-2003 and supports pre-standard IEEE Std. 802.3at-2006™ power requirements.
- Meets IEC 61000-4-2/3/4/5/6 requirements.
- Meets IEC 60950 over-voltage protection requirements.
- Integrated rectification for superior high voltage protection.
- Integrated DC-DC converter provides exceptional EMI performance.
- Programmable DC current limit up to 800 mA.
- Supports “two finger” classification for the proposed standard IEEE Std. 802.3at-2006 higher power PD applications.
- Provides seamless support for local power.
- Over-temperature protection.
- 5x5 mm, 20 lead QFN Package, RoHS compliant.
REFERENCE DESIGN IMPLEMENTATION

BCM5481 IMPLEMENTATION

The BCM5481 consists of a triple-speed 1000Base-T/100Base-TX/10Base-T Gigabit Ethernet transceiver integrated into a single monolithic CMOS chip. The device performs all physical-layer functions for 1000Base-T, 100Base-T, and 10Base-T Ethernet on standard category 5 unshielded twisted pair (UTP) cable. 10Base-T can also run on standard category 3, 4, and 5 UTP. The BCM5481 is a highly integrated solution combining digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders, decoders, echo cancellers, crosstalk cancellers, and all required support circuitry. Based on Broadcom’s proven Digital Signal Processor (DSP) technology, the BCM5481 is designed to be fully compliant with GMII, RGMII, and MII specifications, allowing compatibility with industry-standard Ethernet MACs and switch controllers.

Designed for reliable operation over worst-case category 5 cable, the BCM5481 automatically negotiates with its link partner to determine the highest possible operating speed. The device detects and corrects most common wiring problems. The BCM5481 features CableChecker™ Diagnostics, which detects common cable problems including shorts, opens, and cable length.

The DESIGN implements the RGMII functionality. While any of the interface modes could be used, this mode provides a balance that uses half the clock frequency of the SGMII (lower EMI generation) and fewer signal lines/pins than the MII implementation.

![BCM 5481 Block Diagram](image-url)
AS1602 IMPLEMENTATION

The AS1602 is a single-chip, highly integrated CMOS solution for 10/100/1000 Ethernet applications where EMC Class B compliance is required, along with ESD protection. The AS1602 interfaces directly to Ethernet transformers and enables system designers to meet EMI emissions, EMI immunity, Air Discharge and Cable Discharge design requirements. The AS1602 utilizes Akros Silicon’s patented active EMI suppression technology, which offers superior EMI reduction and immunity, compared to passive filter techniques in Ethernet applications. The adaptive and continuous suppression operates over the entire Ethernet signal bandwidth. In addition, the AS1602 includes highly robust ESD/Surge protection diodes. Built using proprietary design techniques, these diodes are capable of shunting both moderate energy/fast transients that create high thermal stress as well as high energy/slow transient events that create tremendous voltage overstress. At the system level, the AS1602 absorbs the over-voltage transients preventing damage to the Ethernet Phy.

The AS1602 suppresses common-mode noise present in the Ethernet signals and compensates for many variables that are the source of common-mode noise in Ethernet systems. These include: common-mode noise from Ethernet PHY DACs and drivers, variations in Ethernet line signals caused by transformer and passive component mismatches, variations in PC board designs, and different vendor PHY designs.

Each AS1602 provides 2 channels of EMI suppression. Because it supports gigabit Ethernet operation, the DESIGN uses two AS1602 devices.

![Figure 4 AS1602 Block Diagram](image)
AS1124 IMPLEMENTATION

The AS1124 is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE). Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security and Web Cameras, Analog Telephone Adapters (ATA) and Point of Sales Terminals. The AS1124 provides the functions required for power over Ethernet Powered Device (PD) applications.

The AS1124 integrates rectification and protection circuitry, a PD controller, and a DC-DC converter. This high level of integration provides faster response to surge events and limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device. The device is designed to provide a safe low impedance discharge paths directly back to the earth ground, resulting in superior reliability and circuit protection.

AS1124 has been designed to address both EMI emission concerns and surge/over-voltage protection in POE applications. The AS1124 design minimizes transmission of system common-mode noise on to the UTP while providing high immunity to over-voltage and surge events. The DESIGN uses a single AS1124.
REFERENCE DESIGN SCHEMATICS

The schematics show the implement details for the three major components and supporting circuitry: BCM5481 1GBE PHY device and the AS1124 PoE device.

BCM5481 SCHEMATICS

The BCM5481 1GBE PHY is located on Sheet 4 of the schematics. The TRD [0:3] signal pairs interface from the PoE 1GBE Transformer. The RGMII Signals interface directly to the 1GBE MAC interface. The voltage interface is shown on Sheet 5 of the schematics.

AS1124 SCHEMATICS

The AS1124 DC-DC Converter Interface is located on Sheet 3 of the schematics. The PoE 1GBE Transformer center tap signals provide the DC voltage source signal to the AS1124 device. The remaining circuitry for the DC-DC converter is shown on Sheet 3 for reference.

AS1602 SCHEMATICS

The AS1602 devices are located on Sheet 2 of the schematics. The UTP signals interface through the RJ45 interface connector and directly to the PoE 1GBE Transformer. The TRD [0:3] signal pairs interface to the AS1602 devices and the BCM5481 1GBE PHY device.
AS1124- BCM5481 Reference Design

![Diagram of AS1124-BCM5481 Reference Design]

- RJ-45
- XFMR
- BCM5481
- AS1602
- +12V
- AS1124
- SECONDARY DC-DC
- +2.5V
- MDIO
design layout

The PCB layer assignments provide details on PCB Layers, signal routing layers, Ground planes and Power/Ground planes. Impedance information for Differential signal routing and Single-end signal routing is required for PCB Layout.

The PCB Fabrication Vendor provides this detailed information for the PCB Layout. The following information was provided by Merix (www.merix.com) for the 6 Layer PCB Stack-up.

Layer assignments

The PCB Layer Assignments are recommended for a 6 layer PCB design. Below is the recommended PCB Layer Assignment for copper thickness, copper weight, and layer thickness for each PCB layer as shown in Figure 6. The PCB Layers is assigned as follows:

<table>
<thead>
<tr>
<th>Layers</th>
<th>Signal Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1</td>
<td>Signal Routing (Top)</td>
</tr>
<tr>
<td>Layer 2</td>
<td>Ground Plane</td>
</tr>
<tr>
<td>Layer 3</td>
<td>Internal Signal Routing</td>
</tr>
<tr>
<td>Layer 4</td>
<td>Power/Ground Planes</td>
</tr>
<tr>
<td>Layer 5</td>
<td>Ground Plane</td>
</tr>
<tr>
<td>Layer 6</td>
<td>Signal Routing (Bottom)</td>
</tr>
</tbody>
</table>

The PCB stack-up supports Differential Routing at 100 Ohms and Single-Ended Routing at 50 Ohms. The Differential Routing is required for UTP Signals and TRD Signals from the RJ45, to/from the PoE transformer and to/from the 10/100/1000 Ethernet device.

Figure 6 PCB Layer Assignments
The Single-Ended routing is used for high speed clock and digital signals at 50 Ohms.

The Impedance Table for the 6 Layer PCB stack-up is shown in Table 2 for reference. The Differential Routing for external layers (Layers 1 & 6) and internal layers (Layers 3 & 4) have different trace widths and line pitch. The bulk of the Differential Routing will be on external layers, depending on the complexity of the design some routing will be on internal layers.

### Table 2 Impedance Table – 6 Layers PCB Stack-up

<table>
<thead>
<tr>
<th>Layer</th>
<th>Structure Type</th>
<th>Coated Microstrip</th>
<th>Target Impedance (ohms)</th>
<th>Impedance Tolerance (ohms)</th>
<th>Target Linewidth (mils)</th>
<th>Edge Coupled Pitch (mils)</th>
<th>Reference Layers</th>
<th>Modelled Linewidth (mils)</th>
<th>Modelled Impedance (ohms)</th>
<th>CoPlanar Space (mils)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Single Ended</td>
<td>Yes</td>
<td>50.00</td>
<td>+/-5</td>
<td>8.00</td>
<td>--</td>
<td>(2)</td>
<td>8.00</td>
<td>49.32</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Edge Coupled Differential</td>
<td>Yes</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.50</td>
<td>10.00</td>
<td>(2)</td>
<td>4.50</td>
<td>101.31</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Edge Coupled Differential</td>
<td>--</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.00</td>
<td>12.00</td>
<td>(2, 4)</td>
<td>4.25</td>
<td>99.20</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Edge Coupled Differential</td>
<td>--</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.00</td>
<td>12.00</td>
<td>(3, 5)</td>
<td>4.25</td>
<td>99.20</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Single Ended</td>
<td>Yes</td>
<td>50.00</td>
<td>+/-5</td>
<td>8.00</td>
<td>--</td>
<td>(5)</td>
<td>8.00</td>
<td>49.32</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Edge Coupled Differential</td>
<td>Yes</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.50</td>
<td>10.00</td>
<td>(5)</td>
<td>4.50</td>
<td>101.31</td>
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</table>
SUMMARY

The AS1124-AS1602-BCM5481 reference design implements an RGMII that incorporates a power management system for PoE PDs. The design employs devices to minimize signal noise that can corrupt transmitted data and to meet regulatory EMI requirements, along with ESD protection. By using low-power, small footprint, highly robust ESD/Surge protection and programmable CM suppression devices that do not require special heatsinks or other thermal protection, the DESIGN can be used as a reference to enable quick development of higher performance products such as Voice over IP (VoIP) phones, wireless LAN access points, security and web cameras, Analog Telephone Adapters (ATA), and Point of Sales Terminals.

REFERENCES

This section lists any outside references that contain information not included in this document that may aid in understanding this document. Refer to the appropriate document for additional information.

- AS1124 24W, Powered Device with integrated DC-DC Controller, Akros Silicon, Datasheet
- AS1602 Dual Channel IEEE® 802.3 Compliant EMI Suppressor for 10/100/1000 Ethernet Applications, Akros Silicon, Datasheet
- Design Guide for AS1113/AS1124 PoE Powered Devices, Akros Silicon, Application Note AN004
- AS1602 Design Guidelines, Akros Silicon,
- BCM5481 10/100/1000BASE-T Gigabit Ethernet Transceiver, Broadcom, 5481-DS08-R

DEFINITIONS

Definitions for terms used in this document are defined below for reference. Terms and acronyms are listed in this section for reference.

- AN064 Application Note xxx
- EMI Electromagnetic Interference
- ESD ElectroStatic Discharged
- IEC International Engineering Consortium
- IEEE Institute of Electrical and Electronics Engineers
- PD Powered Device

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