



Application Note AN006

Using PoE Powered Devices with a Local Power Supply

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ABOUT APPLICATION NOTE AN006

Application Note AN006 describes the methodology for applying a local power source to PoE devices that incorporate Akros Silicon integrated PD components. This document applies to the entire AS11xx PD family, even though some diagrams may demonstrate concepts using specific Akros components.

The Akros Silicon PD family includes the AS1113, AS1124, AS1130 and AS1135 devices. Refer to www.akrossilicon.com for further details on these and other Akros Silicon components.

GENERAL DESCRIPTION

Power over Ethernet (PoE) has driven the development of a variety of new powered network appliances. To date, the most prevalent has been IP phones that draw power from the network. This has allowed network administrators to provide 'lifeline' service, following the legacy of the analog phone system. PoE has also found widespread usage in security cameras and wireless-access-points (WAP) due to the convenience and economy of connecting these devices into a LAN infrastructure using conventional Unshielded Twisted Pair (UTP) cabling.

The IEEE 802.3af standard defines a means for delivering combined Ethernet data and up to 13W of power over UTP cable, which is commonly used for VoIP and simple security camera applications. The emerging IEEE 802.3at specification will increase the power delivery to levels above 13W and below 30W. The higher power delivery allows the deployment of surveillance cameras with pan-tilt-zoom (PTZ) capability and WAPs that offer the latest in high-speed wireless connectivity.

The widespread use of PoE is a testament to its convenience and economy. Even if network cabling is not yet installed, it is usually more economical to route UTP cable to the various nodes in the walls and ceilings of a building, without requiring 110V line power for each device.

Yet, even with this convenience, there are still a number of applications that require local power delivery. For instance, a VoIP phone may use PoE power for redundancy. The phone can be connected to a wall power adapter, yet utilize PoE as back-up power during a local power failure (or vice versa). There is also the situation where not all Ethernet connections are wired for power.

By also providing the capability to use a wall power adapter, the usage environment for networked appliances is much broader. For instance, a local power connection would still allow a PoE surveillance camera to be installed in a setting where PoE has not yet been deployed. This creates the ability to use all of the existing LAN infrastructure while also providing a ready migration path to PoE.

POWER INSERTION OPTIONS

There are multiple solutions for provisioning local power, each with its own advantages and drawbacks. The designer has a number of options to consider. One of the first decisions is where to apply the local power source in the design. The second is what voltage to apply.

In most cases, appliances will use a traditional wall adapter to inject local power. From a circuit standpoint, it is most convenient to use an AC adapter that will provide a 48V DC output voltage. This level is consistent with the voltage delivered by the PoE system. However, manufacturers often prefer to work with 24V and 12V wall adapter, for cost, safety or other reasons. These lower voltages require additional circuitry to assure proper operation of the PoE appliance.

Although the DC-DC controller is integrated onboard Akros PoE PD devices, auxiliary local power may be applied at one of three external locations, shown in Figure 1:

1. Input to the Powered Device controller
2. Input to the DC-DC converter
3. Powered Device application load point

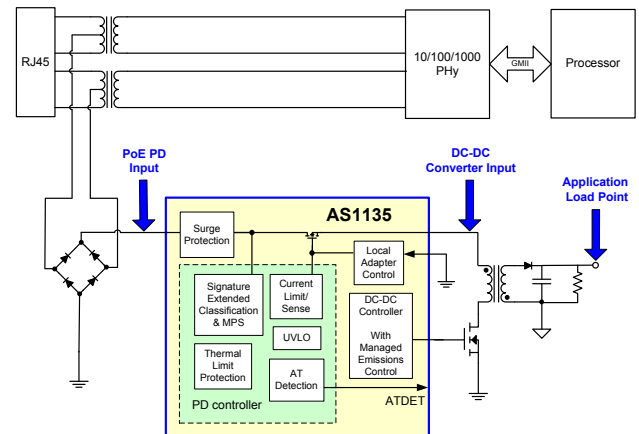


Figure 1 - Local Power Insertion Points

When selecting the insertion point, one must consider both the inrush current and the hand-off sequence. Also, there may be instances when power is applied simultaneously by both the PoE line and the local power source. Generally, local power should be connected to the PD appliance through a diode, to prevent power flow from the PoE line to the wall adapter. Likewise, the diode bridge at the front interface will prevent power flow from the local source back into the PoE line.

INSERTING POWER AT THE POE PD INPUT

Applying power to the input of the PoE PD device through a diode is an option only if the local power source is between 42V and 57V (e.g. 48V wall block supply). Essentially, the PD will treat the local source the same as if were coming from the Ethernet line.

Any input voltage at or above the 42V UVLO threshold (rising edge of V_{IN}), per IEEE® 802.3af/at, will cause the PD controller to close its internal FET switch, allowing power through to the DC-DC converter. This approach has the benefit of using the PD's onboard surge protection and current-limiting circuitry.

If the local source is below the 42V threshold, however, the FET switch might remain open and power will not be passed to the DC-DC converter. AS11XX family PD device full power activation threshold is between 37V and 42V.

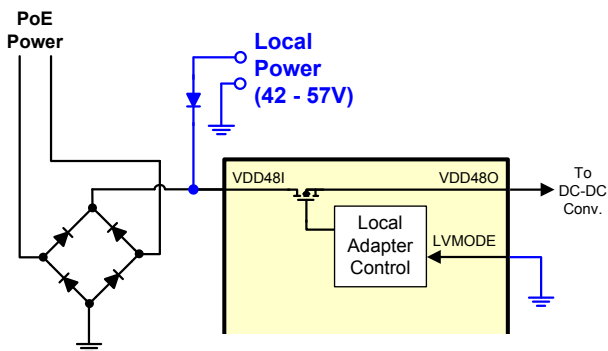


Figure 2 - PoE PD Input Local Power Insertion Using Diode "OR"

As shown in Figure 2 above, local power at the PD input is connected through a diode "OR" with PoE power. Therefore, either supply may power the PD. In the case where both supplies are active, the one with the higher voltage level will be delivered.

The Akros AS1113 and AS1124 chips have onboard diode bridges. With these components, the external diode bridge shown in Figure 2 is not necessary (connect PoE lines directly to pins CT1, CT2, SP1 and SP2). These same components also have an integrated power "OR" function, so local power can be connected directly to V_{AUX} with no external diode.

If the PSE is active and local power is applied that is higher than the PSE voltage, the local power will take over and the current flow from the Ethernet cable will drop below the 5mA Maintain Power

Signature (MPS) minimum threshold (see Appendix A for MPS specifications).

Once the local power supply takes over, the PoE input diode bridge becomes reverse biased and the DC and AC MPS components essentially become disconnected from the circuit. The Power Sourcing Equipment (PSE) at the opposite end of the line will no longer sense a proper power signature load and will stop sending current to the device. The diode bridge will remain reverse biased, preventing the PSE from seeing appropriate detection impedance (Signature resistor and capacitor). If local power is removed, the PSE will go through its normal PoE detection and classification sequence before re-applying power to the device.

Local power may be applied to the device while the PSE is already supplying power, but if it has a lower voltage than the PSE source, it will remain unconnected to the circuit because its input "OR" diode will be reverse biased. The PSE will continue to supply power to the PD.

If the requirement mandates that local power always take priority when available, designers should remember to include diode voltage drops (as well as the range of Ethernet cable lengths) when specifying the minimum local power voltage.

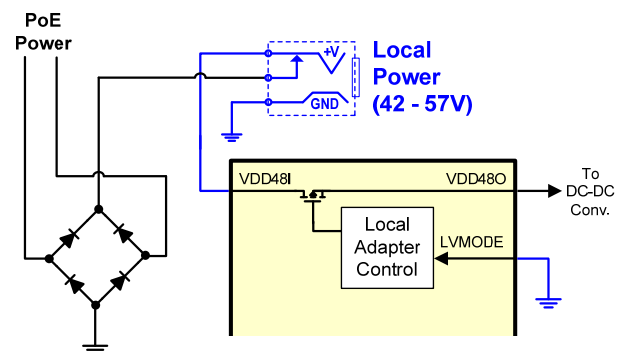


Figure 3 - PoE PD Input Local Power Insertion Using Plug Jack

Another way to fulfill the requirement that local power always take priority is shown in Figure 3 above. Local power is inserted at the PD input through a selector jack. When the local power adapter is not plugged in, the connection is made through the jack to pass PoE power through to the device. When the adapter is plugged in, the PoE connection is broken and local power is passed to the device.

Note: A "break-before-make" plug jack will prevent

local power and PoE power from being connected to the device simultaneously. This also avoids the need for a diode “OR” since local power never has to coexist with PoE power, as is the case in Figure 2.

The plug jack also disconnects the MPS components from the PSE side of the circuit when the adapter is plugged in, so the PSE will see an open circuit and disconnect power. It will not recycle power to the PD until the adapter is physically unplugged from the jack and the MPS components indicate that a valid device is present again.

INSERTING POWER AT THE DC-DC CONVERTER INPUT

The Akros AS11xx PoE PD front end is compliant with the IEEE 802.3af/at Under Voltage Lock-Out limits, which defines that power activation must occur by 42V line voltage, on the rising edge of V_{IN} , and power deactivation must occur by 30V, on the falling edge of V_{IN} . This precludes the use of common 12V and 24V power adapters at the PD input.

Traditionally, applications such as IP cameras and wireless access points have utilized these 12/24V adapters, so as manufacturers migrate their appliances to include PoE functionality, some may prefer to continue using them for cost or legacy.

Low-voltage local adapters can be inserted at the input of the DC-DC controller, as shown in Figure 4. The AS11xx products support this usage mode with a Local Voltage Mode (LVMODE) function. Asserting the LVMODE pin high causes the Local Adapter Control block to disable the internal Hot-Swap FET, which disconnects the incoming Ethernet PoE voltage from the DC-DC converter.

The local power supply can be connected through a diode “OR” (D2 in Figure 4) to the DC-DC controller input without causing contention between the two sources. A simple LVMODE assertion circuit pulls the LVMODE pin high only when local power is present.

The voltage limit for the local power adapter in this mode is dependent on the minimum operating voltage of the DC-DC converter. The Akros AS11xx product family DC-DC controllers are designed to operate with a wide input voltage range of 10-57V while maintaining high converter efficiency.

Low-voltage local power operation requires special design considerations for the power transformer and compensation network. Refer to the section, Transformer Selection for Lower-Voltage Local

Power Source.

Another design consideration is that the insertion of a local power source at the DC-DC converter input bypasses the internal AS11xx surge protection and inrush current control, so designers should make sure that the wall adapter includes appropriate internal protection circuitry.

Designs that insert local power at the DC-DC converter input can utilize a simple LVMODE resistor divider circuit (R1 and R2 in Figure 4) to assert the LVMODE pin in the presence of local power. This assures automatic priority of the local power supply over the PoE supply. Refer to the AS11xx Datasheet for LVMODE pin input thresholds and appropriate resistor divider values, based on the local power supply voltage to be used.

A Zener diode (D1 in Figure 4), is recommended on the LVMODE pin to ensure that $V_{LVMODE} \leq 6V_{max}$ under all transient conditions. To determine the component values in Figure 4, please refer to the device datasheet.

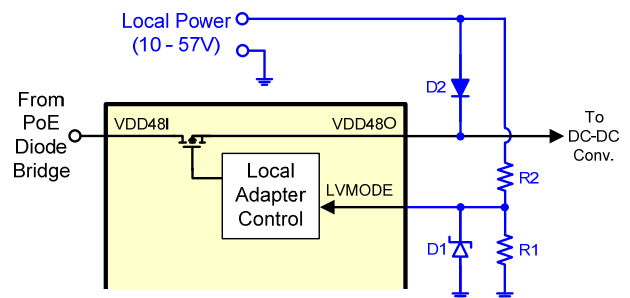


Figure 4 – DC-DC Converter Input Local Power Insertion

Designs that insert local power at the DC-DC converter input and utilize an LVMODE resistor divider circuit will exhibit certain behavior that designers, and possibly device end users, need to understand:

- If PoE power is on and the wall adapter is subsequently plugged in, the LVMODE pin opens the internal Hot-Swap FET switch. The PD will continue to operate exclusively from local power. The PSE may or may not disconnect its power from the device, depending how the PSE implements MPS support. PSE power distribution decisions can be compromised if power continues to be allocated to a PD that now gets its power from a wall adapter.

- If PoE power is on and the wall adapter is subsequently plugged in, then if the PSE properly detects the MPS load drop it will disconnect power. If the wall adapter is later unplugged, the PSE will sense this and restart from the detection stage to re-establish a connection.
- If PoE power is on and the wall adapter is subsequently plugged in, then if there remains a valid MPS, the PSE will stay connected even though the device is drawing power from the wall adapter. Removal of wall adapter power will lower the LVMODE pin, causing the Hot-Swap FET to re-close and the unit will transition back to using the PoE power again.
- If no PoE power is present and the wall adapter is subsequently plugged in, the system will power up immediately from the adapter. Reverse-bias leakage through the Hot-Swap FET will pull up the VDD48I node sufficiently to prevent proper detection of the signature resistance, thereby preventing the PSE from activating. For the PSE to connect successfully with the PD, local power must first be removed (by unplugging the adapter).

Supply source priority in this scheme is also a function of the relative voltages at the diode “OR” output node and will be a function of component tolerances. Ensuring a consistent and defined priority scheme for which of the supplies takes precedence when both are present may require additional components.

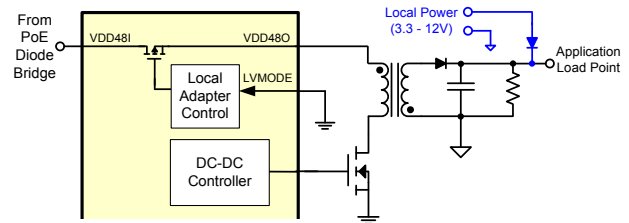


Figure 5 - Application Load Point Power Insertion

INSERTING POWER AT THE DC-DC OUTPUT

The third option for local power insertion is to apply low-voltage wall adapter power directly to the device load, bypassing both the PD controller and the DC-DC converter. Common device operating voltages (e.g. 3.3V, 5V and 12V) require a low-voltage DC wall adapter to match the DC-DC converter output setting. If cleaner board voltage is required, a voltage regulator can be employed at one of several points along the path to the load. Unless protection is built into the wall adapter, this option will not limit inrush current or provide surge protection. Additional protection and output filtering may be required upstream of the device load.

One advantage of applying DC local power at the load is that it is essentially isolated from the PoE PD and DC-DC controller function, downstream of the DC-DC transformer. This should allow the PD to classify, activate the Hot-Swap FET and maintain an MPS current greater than 10mA. The DC-DC converter will remain active, although the load current will be minimal. The drawback is that the efficiency of the DC-DC converter under low load conditions will often fall below 50%, so system energy efficiency will not be optimal.

TRANSFORMER SELECTION FOR LOWER-VOLTAGE LOCAL POWER SOURCE

If the local power voltage and PoE voltage are the same, then there are no additional issues in the transformer design. However, if the local source voltage is significantly lower than the PoE line (<32V), then special consideration must be taken in the transformer circuit design. The primary inductance and turns ratio of the transformer impact the duty cycle for the DC-DC converter.

Fundamentally, the signal at the switching node of the transformer follows the relationship:

$$I_{MEAN} := I_{IN} \cdot \frac{T}{T_{ONCAL}}$$

$$D_{MIN} := V_S \cdot \frac{N}{(V_S \cdot N + V_{INMAX} \cdot N_S)}$$

$$V_{SYN_NEGMAX} := V_{SYN} \cdot \frac{(1 - D_{MIN})}{D_{MIN}}$$

$$\Delta I := V_{INMIN} \cdot \frac{T_{ONCAL}}{L_{CCM}}$$

$$I_{PEAK} := I_{MEAN} + \frac{\Delta I}{2}$$

$$L_{CCM} := \eta \cdot V_{INMIN}^2 \left[\frac{D_{CAL}^2}{(2 \cdot I_{OUT_MIN} \cdot V_S \cdot F_{SW})} \right]$$

In addition, use the following transformer selection guidelines:

- Set the minimum duty cycle, D_{MIN} , to 26-28%.
- Make sure the negative voltage on the Syn winding is less than 18V.
- Set the current ripple to approximately 40-50% of I_{MEAN} to minimize AC loss.
- Design for minimum output current between the boundaries of Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM).

I_{MEAN} = mean primary current during “ON” period

I_{IN} = input current at DC-DC converter

T = switching period of power FET

T_{ONCAL} = theoretically-calculated conduction time during one switching period of power FET

D_{MIN} = duty cycle at minimum load, maximum input voltage

V_S = voltage level at secondary of power transformer (normally one diode drop higher than DC-DC converter output voltage)

N = primary turns

V_{INMAX} = maximum input operating voltage

N_S = secondary turns

V_{SYN_NEGMAX} = absolute max of synchronization FET negative gate drive voltage

V_{SYN} = synchronization FET gate drive voltage

ΔI = ripple current (change of primary current during the “ON” period)

V_{INMIN} = minimum DC-DC converter input voltage

L_{CCM} = primary inductance in continuous conduction mode

I_{PEAK} = primary peak current

η = DC-DC converter efficiency

I_{OUT_MIN} = minimum output current (transformer conduction transition from DCM into CCM)

D_{CAL} = calculated duty cycle

F_{SW} = operating frequency (switching frequency), equal to $1/T$

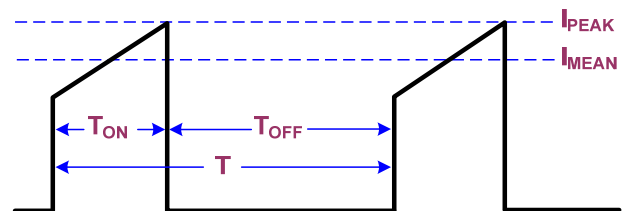


Figure 6 – Theoretical Power Transformer Primary-Current Waveform

Below is a table of transformers suitable for lower-voltage local power designs that have passed Akros Silicon's production-level performance tests. Note: This is not a complete list and omissions are not intended to suggest the unsuitability of other vendors' products.

Table 1 - Tested and Approved Transformers

AKROS PART #	APPLICATION REGULAR PoE INPUT 36-57V	LVMODE OPERATING VOLTAGE RANGE	VENDOR	TRANSFORMER PART #
AS1113	3.3V13W Sync Flyback	10-57	Halo	TGSP-P035EFD15LF
AS1113	3.3V13W Sync Flyback	10-57	Coilcraft	HA3585
AS1113	5V13W Sync Flyback	10-57	Halo	TGSP-P025EFD15LF
AS1113	5V13W Sync Flyback	10-57	Coilcraft	HA3586
AS1135	3.3V30W Sync Flyback	36-57	Halo	TGSP-P027EFD20LF
AS1135	3.3V24.6W Sync Flyback	10-57	Halo	TGSP-P031EFD20LF
AS1135	3.3V24.6W Sync Flyback	10-57	Coilcraft	HA3713
AS1135	5V30W Sync Flyback	36-57	Halo	TGSP-P026EFD20LF
AS1135	5V30W Sync Flyback	36-57	Coilcraft	GA3567
AS1135	5V30W Sync Flyback	10-57	Halo	TGSP-P032EFD20LF
AS1135	5V30W Sync Flyback	10-57	Coilcraft	HA3715
AS1135	12V30W Async Flyback	36-57	Halo	TGSP-P028EFD20LF REV_C

Prior to designing, please contact Akros Silicon for the most recent list of optimized and qualified transformers.

Vendor contact information:

- Halo Electronics
<http://www.haloelectronics.com>
- CoilCraft
<http://www.coilcraft.com/>
- Würth Elektronik Group
<http://www.we-online.com>

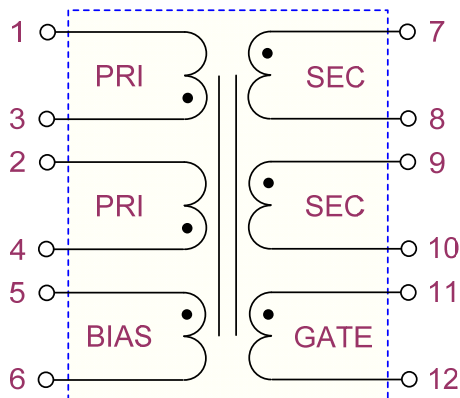


Figure 7 - Example Transformer Pinout

LOCAL POWER USAGE OPTIONS

Table 2 - Local Power Usage Options

PARAMETER	PD INPUT	DC-DC INPUT	DC-DC OUTPUT
V _{AUX} Range	42-57V	10-57V	3.3-12V Broader range can be used with additional switchers.
Power Priority	Diode-Or: Higher Supply prevails. Local Power priority can be implemented through use of special break-before-make plug jack or other circuit.	Local Power using LV Mode feature of the AS11xx family.	Diode-OR: Higher Supply prevails. Additional circuit required to implement defined priority.
PSE Disconnection	PSE disconnects if Local Power is higher or plug jack is used.	PSE may or may not disconnect, depending on PSE DC/AC MPS implementation.	PSE does not disconnect.
PSE Activation	PSE will not activate in presence of local power.	PSE will not activate in presence of local power.	PSE can activate in presence of local power.
Power Transition PSE → V _{AUX}	Smooth transition	Smooth transition	Smooth transition
Power Transition V _{AUX} → PSE	PSE reactivation	PSE may reactivate, depending on PSE connect/disconnect state.	Smooth transition
Magnetics Design	Relatively simple. Smaller sizes achievable.	More complex. Higher output wattage with lower V _{IN} requires larger cores.	Relatively simple
External BOM	Minimal, unless local power priority implementation is required.	Minimal	Will likely require additional separate switchers to match V _{OUT} to the V _{AUX} path.
System efficiency	Excellent	Excellent for PoE. Wide-input-range magnetics will lead to lower system efficiency with low V _{AUX} (12V).	Local Supply usage with powered PD and PWM will impact efficiency.

SUMMARY

Use of wall adapters can increase the versatility of PoE PD appliances. Wall adapters allow operation within legacy Ethernet environments until PoE is deployed. Two independent power sources can also provide redundancy for mission-critical applications.

As demonstrated, there are several methods for local power insertion. Designers should carefully weigh the electrical behavior, BOM cost and performance trade-offs of each before choosing a local power design solution.

Designers can proceed with the confidence that Akros Silicon has a thorough understanding of transformer design and can readily assist customers with the transformer selection and optimization process.

APPENDIX A - IEEE 802.3AF/AT MAINTAIN POWER SIGNATURE SPECIFICATIONS¹

At the start of the detection cycle, the PSE checks both detection signature resistance and parallel detection signature capacitance in order to validate a device that is awaiting power. For the PD to continually receive power from the PSE, it must maintain its power signature so the PSE continues to see a valid load.

MAINTAIN POWER SIGNATURE (MPS)

The MPS consists of two components, the DC MPS and AC MPS. DC MPS refers to the DC current requirement and AC MPS refers to the AC signal response (resistance and capacitance) during AC disconnect detection.

The PSE checks the Maintain Power Signature by one of the following methods:

1. AC MPS – 27k Ω or lower impedance at the PI interface to guarantee connection, and 1.98M Ω or greater to guarantee disconnection.
2. DC MPS -- 10mA DC or greater current drawn from the PSE to guarantee connection and 5mA or less to guarantee disconnection.
3. Both DC MPS and AC MPS tests are performed.

The MPS provided by the PD must meet **all** of the following requirements after successfully being connected by the PSE to PoE power:

- Current draw \geq 10mA (min 25% duty cycle consisting of minimum 75ms ON, maximum 250ms OFF)
- Input resistance \leq 26.25 k Ω
- Input capacitance \geq 0.05 μ F

To save power, IEEE specifications allow for removing current draw 75% of the time. The PD must draw a minimum of 10mA current for at least 75ms, followed by an optional drop in current consumption for no longer than 250ms.

If a PD fails to continually maintain the above characteristics, the PSE may elect to remove power from the device.

GUARANTEED DISCONNECT

A PD that no longer requires power and intends to cause itself to become disconnected from the PSE power must meet **all** of the following requirements:

- Current draw \leq 5mA
- $Z_{AC} \geq$ 1980 k Ω (AC probing frequency range = 5-500Hz)

Therefore, it is recommended that both DC MPS (current) and AC MPS (resistive and capacitive signature components) be electrically removed from the network to guarantee proper DC MPS and AC MPS disconnect (such as by using a relay or select jack).

Removing only the signature resistor is not sufficient to guarantee disconnect, given that some PSE systems elect to test only the AC signature component. Since a minimum 50nF capacitor has a Z_{AC} of 6.4k-636k Ω in the 5-500Hz AC probing range, the PSE will not see the minimum 1980 Ω required to guarantee ACMPS disconnect.

REFERENCE MATERIALS

- IEEE P802.3atTM Specification
- AS1113/24/30/35 Datasheets

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