Application Note AN025

Designing for Wide-range Multi-input PoE PD Systems such as IP Cameras

Rev 0.6
October 2008

PRELIMINARY

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FIGURES AND TABLES

ABOUT APPLICATION NOTE AN025

Application Note AN025 describes how to implement a universal PoE PD system design supporting a wide range of input options, including PoE (36V-57V), 24VAC and 12VDC local/auxiliary power inputs. With minimal bill-of-materials changes only, a single Akros-based design can seamlessly support 13W/30W and 802.3af/at designs operating over a wide input voltage range of 9.5V-57V.

These guidelines should be used in conjunction with the datasheet and reference design. The design guide provides information for adapting the reference design to a customer's system. If there are any questions of concerns, please contact the Akros applications team through your sales contact or sales@akrossilicon.com.

Refer to www.akrossilicon.com for further details on these and other Akros Silicon components.

Status:	Advanced Information	Advance Information: Document contains design specifications for initial product development. Preliminary Information: Document contains preliminary data and will be revised at a later date. Final Information: Document contains specifications on a product that is in final release.
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GENERAL DESCRIPTION

Power over Ethernet (PoE) has found increasing use in a variety of new powered-network appliances. One example of such growth is in the area of IP cameras (see Figure 1). This growth has been driven by the convenience and economy of connecting security cameras into a LAN infrastructure using conventional Unshielded Twisted Pair (UTP) cabling.

The IEEE 802.3af standard defines a means for delivering combined Ethernet data and up to 13W of power over UTP cable, which is commonly used for simple security camera applications. The emerging IEEE 802.3at specification will increase the power delivery to levels above 13W and below 30W. The higher power delivery allows the deployment of surveillance cameras with pan-tilt-zoom (PTZ) capability and housing temperature control for outdoor environments.

Although network cabling is economical and convenient to install, security cameras are still commonly designed to take advantage of established local power delivery infrastructure, such as 24VAC or 12VDC rails. There is also the situation where not all Ethernet connections are wired for power. As such, there is much benefit to utilizing PoE PD designs that can support a variety of input power options, including PoE, 24VAC and 12VDC.

By providing the capability to use a local wall-power adapter, the usage environment for networked appliances is much broader. For instance, a local power connection still allows a PoE surveillance camera to be installed in a setting where PoE has not yet been deployed. Such flexibility allows the use of the existing LAN infrastructure while also providing a ready migration path to PoE.

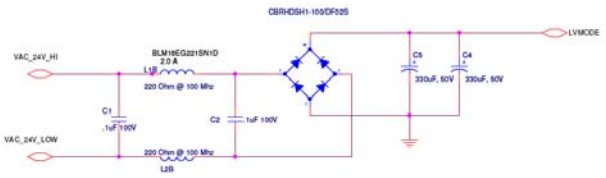
The AS1135 integrated circuit is designed to handle a wide range of input voltages (i.e. 9.5V to 57V) and corresponding DC/DC converter duty cycles with a single system design.

Figure 1 - IP Cameras

LOCAL POWER OPTIONS - 24VAC RECTIFICATION AND 12VDC

Local-power options can be made compatible by using a rectifier circuit to convert 24VAC to ~32VDC (as shown in Figure 2). In such a way, both 24VAC inputs and 12VDC inputs can utilize the same channel for the local power path.

Figure 2 - Rectifier Circuit



For example, if either a 24VAC input or a 12VDC input will be used (but not plugged in at the same time), then either input can be applied to the same input terminals of the rectifier circuit.

On the other hand, if both the 24VAC input and 12VDC input can be simultaneously connected to the system, then an additional diode "OR"ing scheme should be implemented at the output of the diode bridge to merge in the 12VDC option.

PRIORITY SCHEMES FOR MULTIPLE INPUTS – POE VS. LOCAL POWER

Power Mode Selection Using the LVMODE Pin on the AS1135

For the AS1135, the LVMODE pin can be utilized in applications where the PD appliance is designed to draw power from either the Ethernet cable or an external DC local-power adapter. The LVMODE pin is a current-mode input pin, with low and high thresholds as defined in the parametric tables of the AS1135 Datasheet. LVMODE is asserted when the input current exceeds the I_{IH} threshold, and is de-asserted when the input current is below the I_{IL} threshold. If LVMODE operation is not desired, the LVMODE pin should be connected to GND.

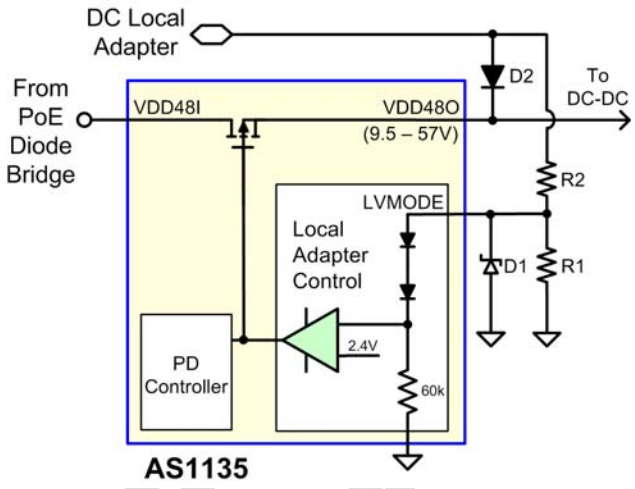
For the systems shown in this application note, primary-side power merging of input sources is shown. For details on configuring other various power insertion options (e.g. primary-side vs. secondary-side merging), please refer to "AN006 - Using PoE PD with a Local Power Supply, Rev. 1.0".

Priority Given to Local Power

Figure 3 shows a simplified internal implementation and external application circuit required to use the LVMODE feature. When power is applied at the local-adapter input, the AS1135 enters Local Voltage Mode. This opens the internal Hot-Swap FET switch while the DC-DC converter is in operation.

In this configuration, local power always takes priority, even in the presence of PoE power, regardless of their relative voltages. If local power is removed, the device will exit Local Voltage Mode operation and PoE power will be used, if available.

Figure 3 - LVMODE Implementation



Local power, whether from a 12VDC source or a rectified 24VAC source, is inserted at the VDD48O node through an external diode (D2). Use of a low reverse-leakage diode is recommended (<350uA, at worst-case temperature). This ensures that when there is no local power, PoE voltage at the VDD48O node will not falsely pull up the LVMODE pin due to high reverse leakage through the diode.

An appropriate ratio of R2 and R1 resistors should be used to ensure proper operation across all supply voltages. Table 1 lists appropriate choices of R2 and R1 resistors to work with a variety of popular local adapter DC voltages. Though a common value of R2 and R1 can be used across the whole range of local supply voltages from 9.5V to 57V, using different value pairs, per the table below, will minimize power consumption. The maximum input voltage at the LVMODE pin should not exceed 6V, therefore a Zener diode (D1) is recommended to limit transient voltage excursions at the pin.

Because the input current at the LVMODE pin defines its state, it is not recommended to drive other circuits or components directly from the LVMODE node (such as an LED) that might draw current. LEDs or current-absorbing components may be driven directly from the Local Supply pin.

Table 1 - LVMODE Configuration

Local Voltage Range	Recommended Local Adapters	R2	R1
9.5V-57V	12V, 18V	2.74kΩ	4.02kΩ
20V-57V	24V, 30V	11.3kΩ	4.02kΩ
32.4V-57V	36V, 48V	20kΩ	4.02kΩ
Diode D1: 5.6V Zener, BZT56V Diode D2: S3B (100V/3A, worst-case reverse leakage <250uA), use of a low reverse-leakage diode with worst-case reverse leakage under high temperature <350uA is recommended.			

The AS1135 internal DC-DC controller is designed to operate with input voltages of 9.5V-57V, to allow applications to take advantage of the LVMODE feature. Besides configuring the device for operation from a local power source, the external power transformer must also be designed to ensure proper operation across the complete input range. Please contact Akros Silicon for system design assistance.

Figure 4 shows the detailed reference schematic for a system implementation supporting PoE, 24VAC and 12VDC inputs, with the local VAC_24V/VDC_12V adapter always given priority.

Priority Given to PoE Power

For systems desiring that priority be given to PoE power when both local power and PoE power are present, an alternate circuit scheme can be used.

The logic in the detailed schematic shown in Figure 5 is designed to give priority to PoE power. If power is applied through the PoE input and the local adapter, the power to the converter always comes from the PoE source. The PoE input drives the gate of the P-channel MOSFET, Q6, so whenever PoE power is applied, Q6 turns off, and the LVMODE pin is pulled low through R7. This keeps the internal Hot-Swap FET (between V48I and V48O) on, thereby applying power from the PoE input to the converter by overdriving the lower local-adapter voltage.

On the other hand, whenever there is no power through PoE, the gate of Q6 is pulled low, causing the P-channel MOSFET (Q6) to turn on, thereby shutting off the internal Hot-Swap FET with power being applied to the converter through the VAC_24V or VDC_12V adapter.

Diode D13 blocks the voltage from LVMODE, as the body diode of the internal Hot-Swap FET allows a direct current path from V48O (anode) to V48I (cathode).

WIDE-INPUT PD SYSTEM SCHEMATICS

For complete system reference schematics and associated bills of materials, please contact Akros Silicon.

Figure 4 - Reference Schematic for 3-input System (PoE, 24VAC and 12VDC) with Local Power Given Priority

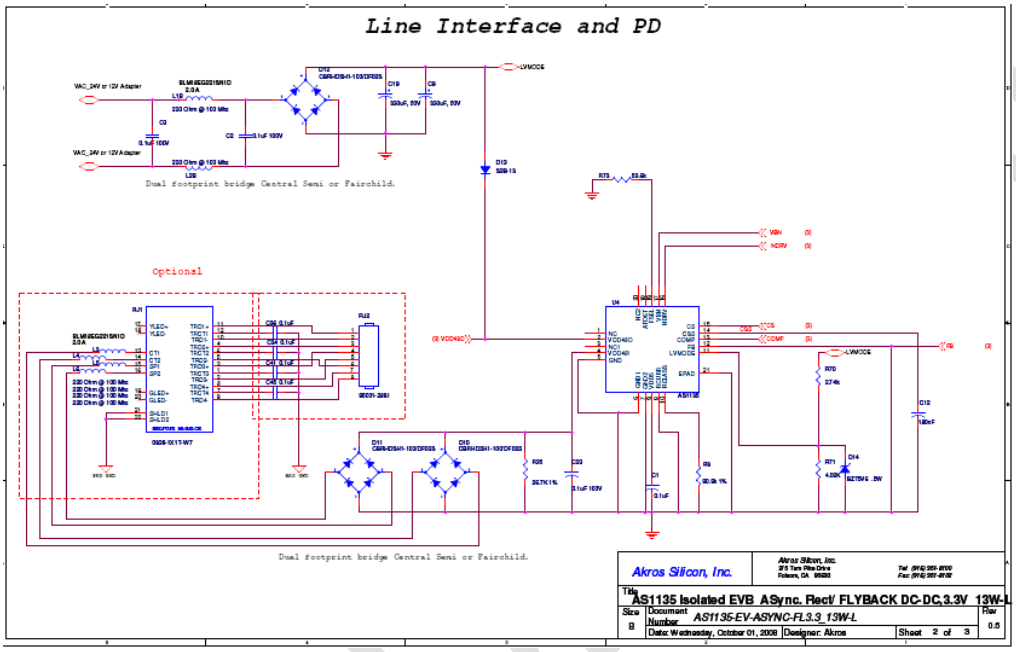
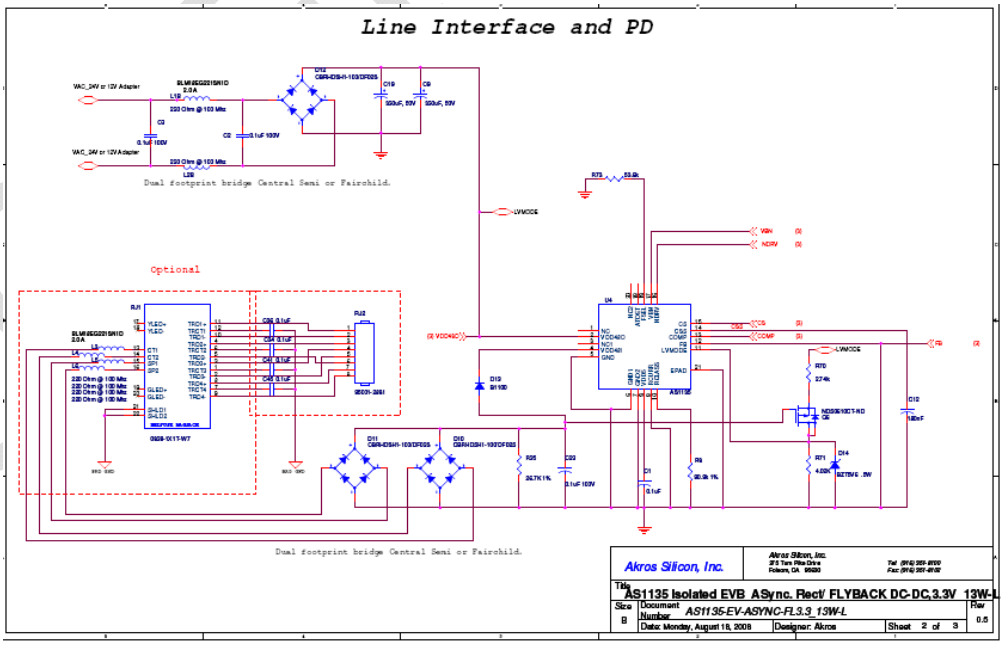


Figure 5 - Reference Schematic for 3-input System (PoE, 24VAC and 12VDC) with PoE Power Given Priority



TRANSFORMER SELECTION FOR LOWER-VOLTAGE LOCAL POWER SOURCE

If the local-power voltage and PoE voltage are the same, then there are no additional issues in the transformer design. However, if the local source voltage is significantly lower than the PoE line (<32V), then special consideration must be taken in the transformer circuit design. The primary inductance and turns ratio of the transformer impact the duty cycle for the DC-DC converter.

Fundamentally, the signal at the switching node of the transformer follows the relationship:

$$I_{MEAN} := I_{IN} \cdot \frac{T}{T_{ONCAL}}$$

$$D_{MIN} := V_S \cdot \frac{N}{\left(V_S \cdot N + V_{INMAX} \cdot N_S\right)}$$

$$V_{SYN\_NEGMAX} := V_{SYN} \cdot \frac{\left(1 - D_{MIN}\right)}{D_{MIN}}$$

$$\Delta I := V_{INMIN} \cdot \frac{T_{ONCAL}}{L_{CCM}}$$

$$I_{PEAK} := I_{MEAN} + \frac{\Delta I}{2}$$

$$L_{CCM} := \eta \cdot V_{INMIN}^{\,2} \left[\frac{D_{CAL}^{\,2}}{\left(2 \cdot I_{OUT\_MIN} \cdot V_S \cdot F_{SW}\right)} \right]$$

In addition, use the following transformer selection guidelines:

- Set the minimum duty cycle, D_{MIN}, to 26-28%.
- Make sure the negative voltage on the Sync winding is less than 18V.
- Set the current ripple to approximately 40-50% of I_{MEAN} to minimize AC loss.
- Design for minimum output current between the boundaries of Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM).

I_{MEAN} = mean primary current during "ON" period

I_{IN} = input current at DC-DC converter

T = switching period of power FET

T_{ONCAL} = theoretically-calculated conduction time during one switching period of power FET

D_{MIN} = duty cycle at minimum load, maximum input voltage

V_S = voltage level at secondary of power transformer (normally one diode drop higher than DC-DC converter output voltage

N = primary turns

V_{INMAX} = maximum input operating voltage

N_S = secondary turns

$V_{SYN-NEGMAX}$ = absolute max of synchronization FET negative gate drive voltage

V_{SYN} = synchronization FET gate drive voltage

ΔI = ripple current (change of primary current during the "ON" period)

V_{INMIN} = minimum DC-DC converter input voltage

L_{CCM} = primary inductance in continuous conduction mode

I_{PEAK} = primary peak current

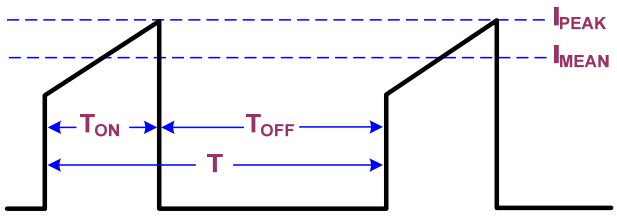
η = DC-DC converter efficiency

$I_{OUT-MIN}$ = minimum output current (transformer conduction transition from DCM into CCM)

D_{CAL} = calculated duty cycle

F_{SW} = operating frequency (switching frequency), equal to 1/T

Figure 6 - Theoretical Power Transformer Primary-Current Waveform



Below, in Table 2, is a list of transformers suitable for lower-voltage local power designs that have passed Akros Silicon's performance tests. Note: This is not a complete list, and omissions are not intended to suggest the unsuitability of other vendors' products.

Prior to designing, please contact Akros Silicon for the most recent list of optimized and qualified transformers.

Table 2 - Approved LVMODE Transformers

AKROS PART #	APPLICATION	LVMODE OPERATING VOLTAGE RANGE	VENDOR	TRANSFORMER PART #
AS1135	3.3V13W Sync Flyback	10-57	Coilcraft	HA3585-BL
AS1135	3.3V13W Async Flyback	10-57	Halo	TGP13-S032EP13LF
AS1135	5V13W Sync Flyback	10-57	Halo	TGSP-P025EFD15LF
AS1135	5V13W Async Flyback	10-57	Coilcraft	HA3871-AL
AS1135	3.3V30W Sync Flyback	10-57	Coilcraft	HA3809-AL
AS1135	5V30W Sync Flyback	10-57	Halo	TGSP-P032EFD20LF
AS1135	5V30W Sync Flyback	10-57	Coilcraft	HA3715-DL

Vendor contact information

- Coilcraft, Inc.
  http://www.coilcraft.com
- Halo Electronics, Inc.
  http://www.haloelectronics.com
- Pulse Engineering, Inc.
  http://www.pulseeng.com
- Würth Elektronik Group
  http://www.we-online.com

Additional Reference Material

- IEEE P802.3at™ Specification
- AS1135 Datasheet
- AN006 - Using PoE PD with a Local Power Supply
- AN024 - AS1135 Universal Reference Design

SUMMARY

Use of local-power adapters can increase the versatility of PoE PD appliances. Such adapters allow operation within legacy Ethernet environments until PoE is deployed. In addition to configuration flexibility, multiple independent power sources can also provide redundancy for mission-critical applications.

The Akros AS1135 integrated circuit delivers a "one size fits all" PoE PD solution, enabling easy forward and backward design compatibility as well as maximum flexibility in supporting a wide range of applications (802.3af/at, 13W/30W and 9.5-57Vin). With a single design enabling such a wide range of applications with only a few bill-of-material loading option changes, time to market is greatly improved, especially as a viable "copy-paste" design approach can be employed.

Finally, designers can proceed with confidence that Akros Silicon has a thorough understanding of transformer design and can readily assist customers with the transformer selection and optimization process.

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