Application Note AN60

AS160X Design Guide

Revision 1.5
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Preliminary Information subjected to future revision and changes

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The AS160X family refers to the footprint compatible parts AS1601 and AS1602. The AS1601 is a single-chip, highly integrated CMOS Active EMI Suppressor for Common-Mode Noise suppression in 10/100/1000 Ethernet applications where compliance to tougher EMI Emissions (Class B) and EMI Immunity standards (Level 3 or higher). The AS1602 includes the AS1601 EMI suppressor and an ESD/transient voltage suppressor. Applications include compliance to IEC61000-4-2 Air/Contact Discharge protection (±25kV Air Discharge), as well as Cable Discharge Events protection (±12kV CDE) in addition to above EMI standards.

This design guide refers to AS1602 as the superset of both AS1601 and AS1602 devices. Same fundamental design and usage considerations are applicable to both AS1601 and AS1602 devices.

System Design Considerations

AS1602 Placement

The AS1602 is designed to be placed between the Ethernet transformer and the Ethernet Phy for providing both ESD protection and CM/EMI suppression on the differential data lines.

The pinout of the AS1602 is designed to mate closely with Ethernet magnetics for ease of board design. The AS1602 should be placed physically near the Ethernet transformer or Mag-jack for optimal EMI performance. This layout facilitates a very low inductance connection between the transformer and the AS1602 that is critical for ESD performance.

Placement of the AS1602 on the same side of the PC-board as the transformer and the Phy is recommended to avoid vias on the Ethernet traces. The AS1602 should be placed such that pin 1 is facing the transformer or mag-jack.

For good Ethernet electrical performance, especially return loss, trace length between the Ethernet Phy and Line transformer should be minimized. See Return Loss Design Considerations section below for detailed design recommendations, and the Akros AN63 application note for detailed analysis.

Power & Ground Connections

The AS1602 shunts common-mode noise to the local ground plane, preventing common-mode noise from being transmitted towards RJ45 and lowering emissions in the system. This requires a very low impedance (DC and RF) connection of AS1602 ground to Ethernet Phy ground (which is usually the same as main board ground). A solid ground plane should be utilized to connect the AS1602 device to rest of the system ground. There should be no slots (direct or due to vias/connector-dots) in the ground plane between the noise generation section (processors and phy) and the AS1602 ground connections. Multiple vias should be used to make connection of GND pins to the ground plane. Ground planes under the transformer should be stitched at electrically short distances (quarter of an inch or smaller).

AS1602 uses a standard 2.5V or 3.3V supply for VDD pins. AS1602 contains high performance analog circuits and use of appropriate power supply filtering and decoupling is recommended. Application schematic in Figure 1 below shows recommended components. General recommendation is to NOT use power plane fill between Phy and Transformer area, instead provide ground fill on the power plane. Hence VDD connection for AS1602 can be routed as wide traces, similar to center-tap VDD of the transformer.

Ethernet Signal Polarity Interchangeability

The AS1602 extracts only the common-mode component of the Ethernet signals for processing. As a result, the polarity of the Ethernet differential pair signal connections to the AS1602 does not matter. This flexibility allows system designers to connect either the positive or negative polarity Ethernet signals to either the TRDnA or TRDnB pins to minimize the use of vias or signal swapping.

Ethernet Signal Feed-Thru Routing

AS1602 is packaged to allow feed-through routing of the Ethernet differential pairs. As described in the AS1602 datasheet, only one side of the package's pins (1, 2, 7 and 8) are internally electrically connected to the EMI Suppression circuitry. Mirrored pins (16, 15, 10 and 9 respectively) are given the same name to enable easy feed-through routing in PC-board design tools.

Functional Control Modes

Mode control description

The AS1602 has several modes of operation. By changing "HBW", "HGM" and "EXRES" settings the AS1602 will accommodate different working conditions and requirements. There are three variables which can be used to make these changes. Pin "HBW" can be set to high or floating to change the performance of common mode (CM) rejection. Pin "HGM" can be set to floating or low state to change the power consumption while maintain the CM rejection performance. Pin "EXRES" can be tied to external resistor of different values to change circuit performance and power consumption.

Below section describes in detail 5 possible operating modes of the device that allow for trade-off between performance and power consumption.

Please note that as described in AS1602 datasheet, HBW=high setting should be used with extreme caution and only when necessary. This increases the loop bandwidth of internal control circuit. Since there are very wide-range of Ethernet transformers, increasing the bandwidth may cause marginal loop stability and oscillations. Though no issues have been found in testing with Akros developed reference designs, due to wide-range of available transformers, this operating mode can not be guaranteed. System designers should test the system to make sure no undesirable common-mode oscillations occur in the system.

Data shown in tables below is with respect to Pulse H5007 POE-compliant GbE transformers (3-cores per signal pair). All CMRR measurements are taken relative to this transformer.

Working Modes

Mode 1: Default mode

Mode 1 is the default working mode. Under typical working condition, AS1602 should give 13dB additional common mode rejection @100MHz and the current will be 49mA.

Following settings are needed to work in mode 1:
HBW = floating
HGM = floating
EXRES = 8.06kΩ for 2.5V or 10.7kΩ for 3.3V power supply.

Table 1 lists the average test results from multiple units, including current from each supply. Total power consumption, common mode rejection with AS1602 and without AS1602, and net decibel common mode rejection AS1602 brings into the system are included. The best operating condition to achieve 13dB common mode rejection is marked in bolded blue in the table. It is achieved at VDD = 2.5V, and VCT = 1.8V, which has the lowest power consumption under default mode, typical 88mW.

Table 1: Average performance of AS1602 under default working mode

HGM	HBW	VDD (V)	VCT (V)	IDD (mA)	ICT (mA)	Power (mW)	CMMR (off)	CMMR (on)	AS1602 CMMR
Z	Z	3.3	3.3	4.97	43.80	161.01	-43.99	-57.25	13.26
Z	Z	3.3	1.8	4.97	43.10	94.03	-43.99	-57.20	13.21
Z	Z	2.5	2.5	4.97	42.30	118.18	-43.97	-57.09	13.12
Z	**Z**	**2.5**	**1.8**	**4.97**	**42.03**	**88.12**	**-43.98**	**-57.05**	**13.07**

Note: "z" means floating pin

Mode 2: Low power mode

The Low Power mode allows system designers a trade-off between power consumption and performance. In this mode, the common mode rejection could be sacrificed by 1dB by reducing the power consumption by about 40%. The typical common mode rejection will be 12dB @ 100MHz under low power mode and the current will be 28mA typically, leading to 52mW typical power consumption with Vdd=2.5/Vct=1.8V setting.

The following settings are needed to work in mode 2.
HBW = floating
HGM = low (tie to ground through 10KΩ pull-down resistor)
EXRES = 8.06kΩ for 2.5V or 10.7kΩ for 3.3V power supply.

When VDD = 2.5V and VCT = 1.8V, the chip has the lowest power consumption under low power mode. It is 52mW typical, marked bolded blue in Table 2.

Table 2: Average performance of AS1602 under low power mode

Operating setup				Performance data					
HGM	HBW	VDD (V)	VCT (V)	IDD (mA)	ICT (mA)	Power (mW)	CMMR (off)	CMMR (on)	AS1602 CMMR
0	Z	3.3	3.3	4.97	22.83	91.80	-43.98	-56.65	12.66
0	Z	3.3	1.8	4.97	22.50	56.91	-43.99	-56.49	12.50
0	Z	2.5	2.5	4.97	22.03	67.49	-43.96	-56.41	12.45
0	**Z**	**2.5**	**1.8**	**4.97**	**21.97**	**51.91**	**-43.98**	**-56.41**	**12.43**

Mode 3: High bandwidth mode

Device CMRR performance can be increased further by increasing the bandwidth of common-mode control loop without increasing the power consumption, by setting HBW=High. This mode may not be usable with all Ethernet transformers and may cause common-mode oscillations. Though no issues have been found in testing with Akros developed reference designs, due to wide-range of available transformers, this operating mode can not be guaranteed. System designers should test the system to make sure no undesirable common-mode oscillations occur in the system. This mode should be used ONLY if it's highly important to increase system performance without increase in power consumption.

This mode allows increase in CMRR performance by +1dB without any penalty in power-consumption. In this mode, at typical working condition, AS1602 should give 14dB additional common mode rejection @100MHz and the current will be 46mA.

The following settings are needed to work in mode 3.
HBW = high (tie to power through 10KΩ pull-up resistor)
HGM = floating
EXRES = 8.06kΩ for 2.5V or 10.7kΩ for 3.3V power supply.

When VDD = 2.5V and VCT = 1.8V, the chip has the low power consumption under high bandwidth mode. It is 87mW typical, marked bolded blue in Table 3.

Table 3: Average performance of AS1602 under high bandwidth mode

Operating setup				Performance data					
HGM	HBW	VDD (V)	VCT (V)	IDD (mA)	ICT (mA)	Power (mW)	CMMR (off)	CMMR (on)	AS1602 CMMR
Z	1	3.3	3.3	6.17	39.83	151.80	-43.99	-57.90	13.91
Z	1	3.3	1.8	6.17	41.03	147.70	-43.98	-58.01	14.04
Z	1	2.5	2.5	6.17	40.03	115.53	-43.97	-57.94	13.98
Z	**1**	**2.5**	**1.8**	**6.17**	**39.83**	**87.09**	**-43.99**	**-57.90**	**13.91**

Mode 4: High bandwidth, Low Power Mode

Mode 4 can be used if the default performance is required under tight power budget in the system. Typical common mode rejection is 13dB at 100MHz and the current will be 26mA. Like the above high bandwidth mode, this mode may not be usable with all transformers and same caution applies as in high bandwidth mode. This mode allows system designers the flexibility of maintaining same performance as default mode with lower power consumption.

The following settings are needed to work in mode 4.
HBW = high (tie to power through 10KΩ pull-up resistor)
HGM = low (tie to ground through 10KΩ pull-down resistor)
EXRES = 8.06kΩ for 2.5V or 10.7kΩ for 3.3V power supply.

When VDD = 2.5V and VCT = 1.8V, the chip has the lowest power consumption under mixed mode while keeping 13dB common mode rejection. It is 52mW typical, marked bolded blue in Table 4.

Table 4: Average performance of AS1602 in High BW, Low Power mode

Operating setup				Performance data					
HGM	HBW	VDD (V)	VCT (V)	IDD (mA)	ICT (mA)	Power (mW)	CMMR (off)	CMMR (on)	AS1602 CMMR
0	1	3.3	3.3	6.17	24.80	102.39	-43.98	-57.04	13.06
0	1	3.3	1.8	6.17	21.40	58.92	-43.99	-57.33	13.34
0	1	2.5	2.5	6.17	20.80	67.50	-43.97	-57.18	13.20
0	**1**	**2.5**	**1.8**	**6.17**	**20.73**	**52.72**	**-43.98**	**-57.18**	**13.19**

Mode 5: High Performance Mode

The High Performance mode can be used additional CMRR performance is desired in the system to combat EMI. This mode is achieved by lowering the value of EXRES resistor to increase the bias current in the system. CMRR performance is improved by over 2dB at 100MHz with ~45% increase in the power consumption. This mode allows the system designers the flexibility of improving system performance with hardware level programmability.

The following settings are needed to work in mode 5.
HBW = floating
HGM = floating
EXRES = 5.49kΩ for 2.5V or 7.32kΩ for 3.3V power supply.

When VDD = 2.5V and VCT = 1.8V, this mode provides 15dB of common-mode rejection for 129mW of power consumption as shown in Table 5 below.

Table 5: Average performance of AS1602 in High Performance mode

Operating setup				Performance data					
HGM	HBW	VDD (V)	VCT (V)	IDD (mA)	ICT (mA)	Power (mW)	CMMR (off)	CMMR (on)	AS1602 CMMR
Z	Z	3.3	3.3	6.7	64.4	234.4	-43.8	-59.0	15.2
Z	Z	3.3	1.8	6.7	63.6	136.5	-43.8	-59.1	15.3
Z	Z	2.5	2.5	6.7	62.7	173.5	-43.8	-58.9	15.1
Z	**Z**	**2.5**	**1.8**	**6.7**	**62.4**	**129.0**	**-43.8**	**-58.8**	**15.0**

Summary of the Operating Modes

There are three pins of AS1602 that affect the total power consumption, HBW, HGM, and EXRES. This allows system designers flexibility and tradeoffs in meeting power/performance requirements of the system.

Users of AS1602 have to refer to the VCT voltage required by the Ethernet Phy and select appropriate operating mode. Note that one has to keep VDD>=VCT.

Table 5 summarizes all above modes under lowest power operating mode – Vdd=2.5V/Vct=1.8V.

Table 6: Summary of Avg performance of AS1602 at Vdd=2.5V/Vct=1.8V

Mode	HGM	HBW	Power (mW)	CMRR	Power Savings	CMMR Gain
Default	Z	Z	88	13	0	0
Low Power	0	Z	52	12	40%	-1dB
High BW	Z	1	88	14	0	+1dB
High BW, Low Power Mode	0	1	52	13	40%	0dB
High Performance Mode (Using 5.49kΩ for EXRES)	Z	Z	129	15	-45%	+2dB

Return Loss Design Considerations

The AS1602 is designed to provide low capacitance loading on the line to have low impact to Ethernet electrical performance, like return loss. Return Loss is a function of Transformer design (leakage inductance and differential parasitic capacitance), Phy output capacitance, trace routing capacitance including any additional components.

Detailed analysis and simulation of return loss performance is discussed in Akros' Application Note AN63. As shown in the AN63 document, AS1602 can be used with appropriate transceiver and transformers to meet Ethernet return loss requirements.

Given a number of system parameters that impact return loss, it's not always possible to predict the performance and variation due to used components. It is recommended that additional ferrite beads be used as means of tuning the return loss performance at system level.

Ferrite Bead Implementation

As discussed in Akros Application Note AN63, the range of inductance needed to tune return loss is between 10-90nH. This can be implemented using widely available ferrite beads which are much more inexpensive than equivalent inductors and are available in small footprints. For selected ferrite beads in the frequency range of interest (<100Mhz), the real part of the impedance is negligible. In out-of-band (beyond 100MHz), the real part of the bead's impedance actually creates a low-pass filtering effect that helps filter out high-frequency harmonics and improves EMI performance.

An appropriate choice of ferrite beads is the Murata BLM18B series (0603), which is meant for high speed signal lines with low DCR values. Ferrite beads are typically rated with impedance rating at 100MHz. Based on AN63 simulations, the range of usable ferrite bead impedance is 10Ω to 47Ω, with good centering at the 22Ω value (BLM18BA220SN1 or BLM18BB220SN1). These beads are also available in the smaller 0402 size (BLM15B series).

Link for Murata catalog is shown below. Note that equivalent models from other vendors can also be used.

http://search.murata.co.jp/Ceramy/image/img/PDF/ENG/L0110S0100BLM18B.pdf

There are two additional considerations associated with the use of Ferrite beads:

- Use of ferrite bead creates a low-pass filter (with 3-db cutoff frequency beyond 100MHz pass-band) that can help remove some of the high frequency harmonics

from transmission on the UTP. This provides significant HF EMI suppression beyond 200MHz range and improves overall system EMI performance.

- Use of ferrite bead can marginally slow down rise/fall time of the Ethernet signal. For the values of ferrite bead considered here, this will typically be in the 100pS range. Given 3-5nS rise/fall time requirements in Ethernet Template, this will have a minimal impact.

Layout & Design Guide

The following is the consolidated design recommendation for designing a media interface to meet return loss requirements.

1. For robust system ESD performance, the AS1602 should be placed as close as possible to the Ethernet transformer with very low inductance connection to the power planes.
2. Place all MDI signal path components on same board side to avoid vias. Vias cause impedance discontinuity and can impact return loss. If vias can not be avoided, match the number and position of vias on each member within MDI signal pair. This is more of an issue for GbE that has more stringent return loss requirements. Note that the AS1602 package is designed to allow through routing that eliminates via drops.
3. Use controlled impedance, microstrip traces with solid ground under signal traces. Each of the MDI differential ("+" and "-") traces should have a 50-ohm characteristic impedance to ground, 100 ohms between each other, and trace lengths matched within 50 mils.
4. Place the components as close together as mechanically possible to minimize differential signal lengths. Always place Ethernet termination resistors (50Ω) very close to the transceiver.
5. Use the transformer as recommended by the transceiver vendor. Transformers with chokes on the line side (towards RJ45) will have better return loss performance. However please review the transceiver-transformer compatibility guide provided by the transceiver vendor, to make sure such transformer is usable.
6. Place recommended ferrite beads on the differential signals between AS1602 and the Ethernet transceiver. Locate the ferrite beads near the transceiver, after the Ethernet termination resistors.
7. In the lab, test for return loss, pulse templates and high frequency EMI noise to fine-tune the value of ferrite bead. For better EMI performance, use the largest ferrite bead (within 10-47Ω range) that allows the system to pass return loss and does not impact the pulse template. Note that if the layout is really compact, ferrite beads may not be needed and can be replaced with 0Ω stuff option or designed out in a later board rev.
8. For GbE: the spacing between the channels controls the inductive crosstalk and should be at least twice the spacing between the members of each pair in a channel.

Typical Application Diagrams

Fast Ethernet (10/100Base-T) Application Diagram

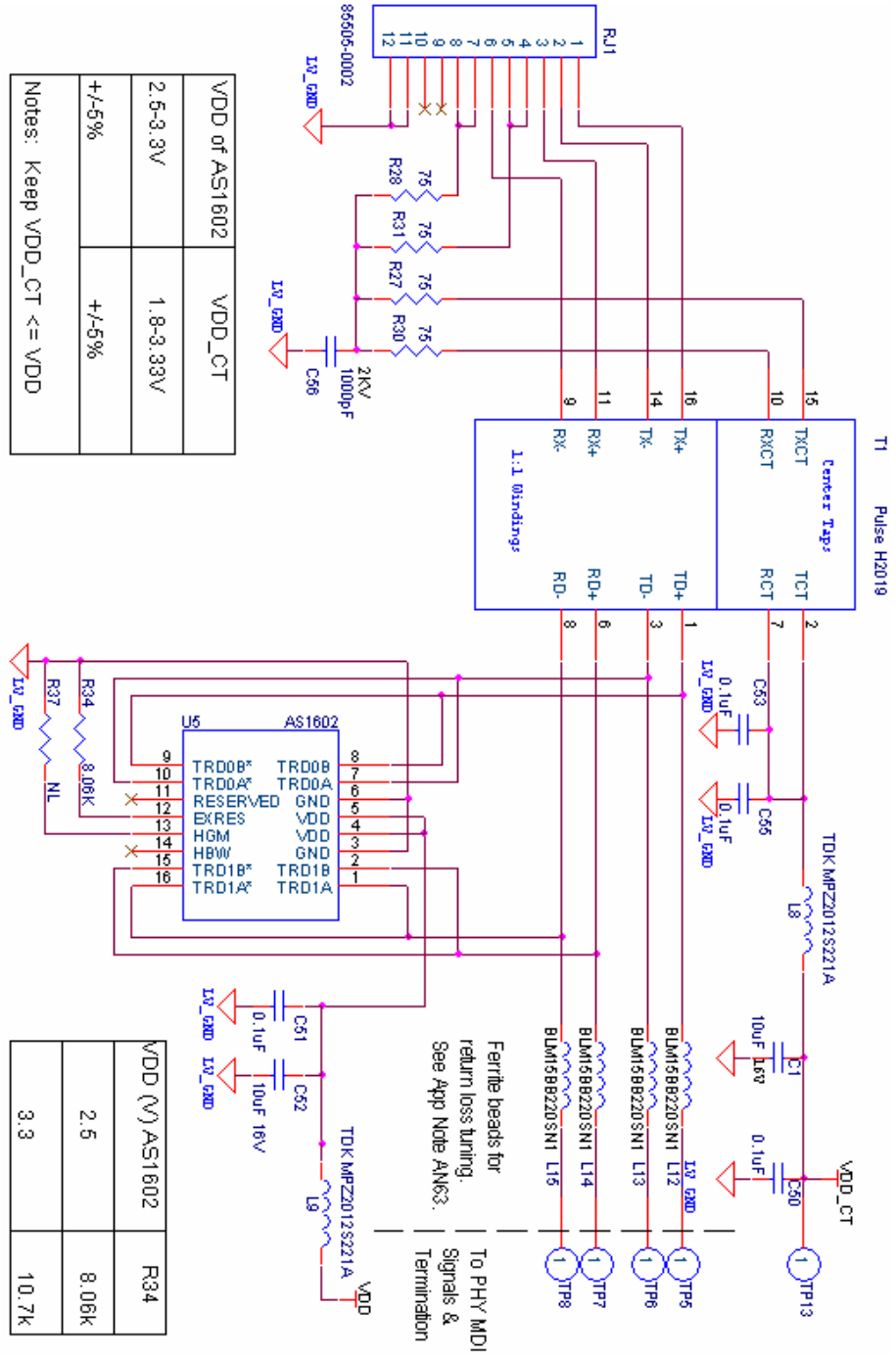

Figure 1: FE Application Diagram using AS1602

Gigabit Ethernet (10/100/1000Base-T) Application Diagram

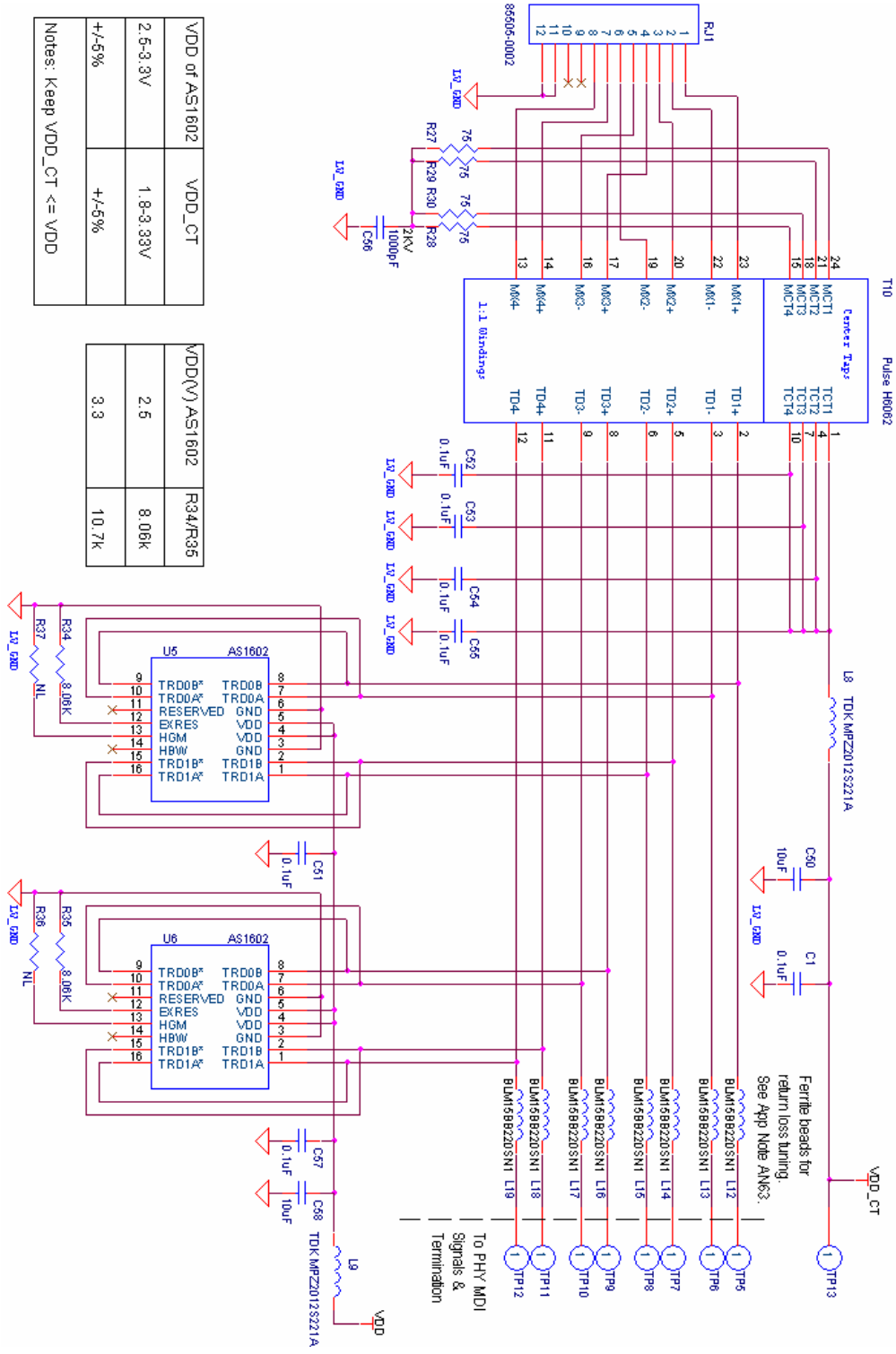

Figure 2: GbE Application Diagram using AS1602

If there are any questions about this implementation, please contact Akros Silicon.

Sample Reference Design for GbE Application

In this sample reference, the analysis was done for a particular customer. The main problem the customer faced was an EMI issue, which was a roadblock to getting EMI Class B certification, and also needed additional ESD protection to meet IEC61000-4-2 Level3 requirements.

The customer had Ferrite Beads between PHY and Ethernet transformer. The Ethernet transformer center tap was 1.8V, decoupled with 0.1uF capacitors on each tap, total 4 center taps. PHY was powered with 3.3V. Then how to implement AS1602 into the existing customer system to improve system level EMI?

Following are the recommendations. Please refer to Figure 2 as the baseline typical application diagram for AS1602 usage in GbE Application.

1. AS1602 to be placed between the Ethernet transformer and the Ferrite Bead.
2. Continue to use VDD_CT = 1.8V for the Ethernet transformer center tap. The VDD_CT has to be in the range of (1.8V~3.3V) which -/+5% tolerance, please keep VDD_CT not higher than VDD of AS1602 at any time.
3. Recommend that VDD_CT be filtered with one ferrite bead and one bulk cap 10uF locally near the transformer center tap.
4. Note that each AS1602 channel will draw about 20mA current from the transformer center tap supply, or 80mA per GbE port (2 pieces of AS1602). Please size ferrite bead and power supply accordingly. 90% of the power consumed by AS1602 is from transformer center tap supply.
5. AS1602 can be used with either 2.5V or 3.3V VDD. Since PHY transceiver is using 3.3V, that supply can be extended for VDD of AS1602. Please also note, VDD is not the same as VDD_CT in this case. And R34 = R35 = 10.7kΩ for biasing.
6. All four AS1602 VDDs can share the same supply filter and bulk capacitor, L9/C58 in Figure 2.
7. A pull-down stuff option on HGM pins of A1602 is recommended for programming. 10KΩ resistor to GND is appropriate, with default of no load.
8. Figure 3 shows actual layout of Figure 2 in GbE application. As seen, the AS1602 pinout has been designed for very clean and through routing of Ethernet signals so that the addition of the AS1602 footprint does not create any stubs on the Ethernet signals.

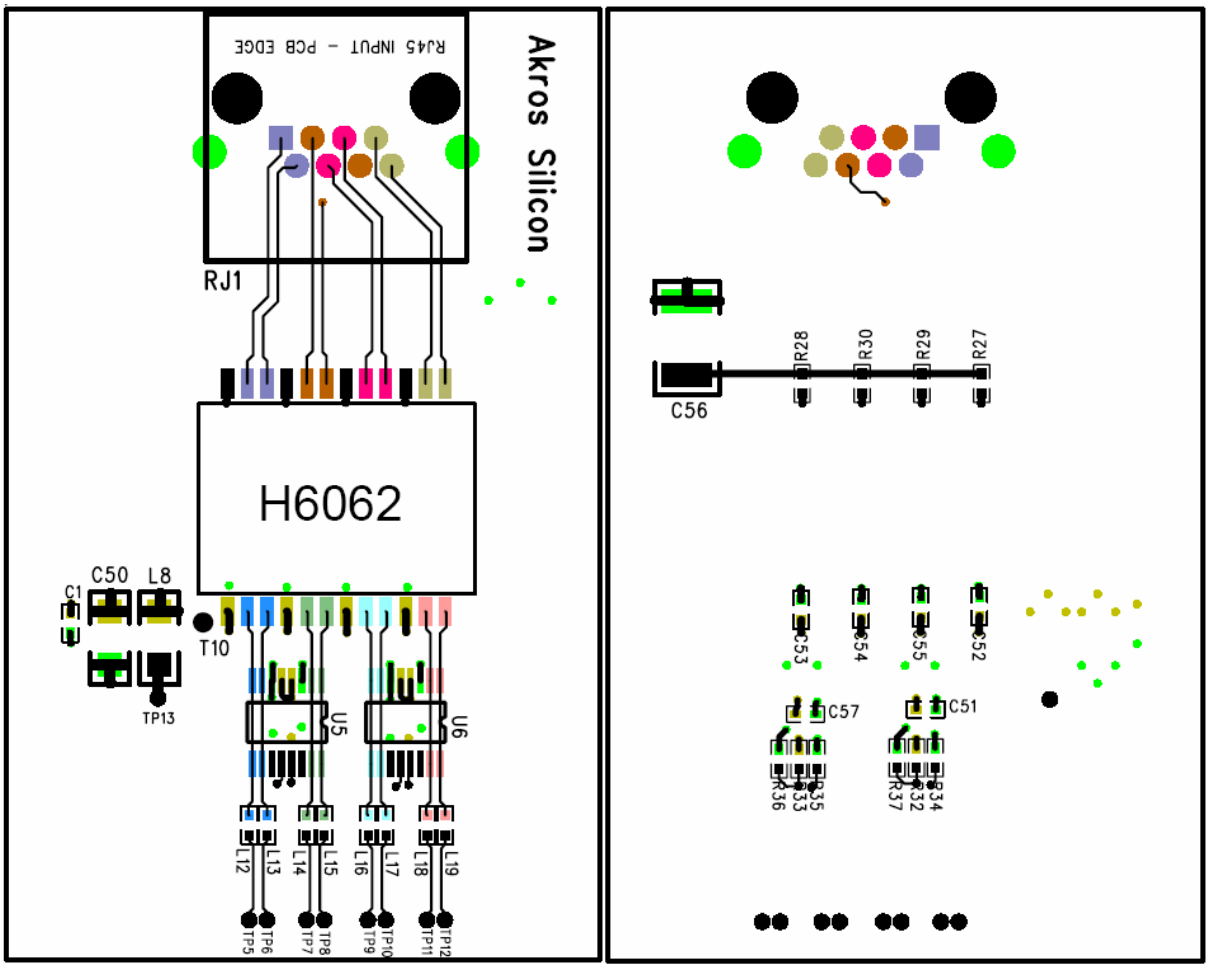

Figure 3a: PCB Top Side Figure 3b: PCB Bottom Side

Figure 3: Layout of Figure 2 in GbE application

Related Documentation

1. Akros Silicon Datasheet: AS1602 Datasheet
2. Akros Silicon Application Note: AN63 – Meeting Ethernet Return Loss with AS160X
3. Murata Datasheet: Noise Suppression Products – EMI Suppression Filters, L0110S0100BLM03A
4. App_layout, Akros

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