

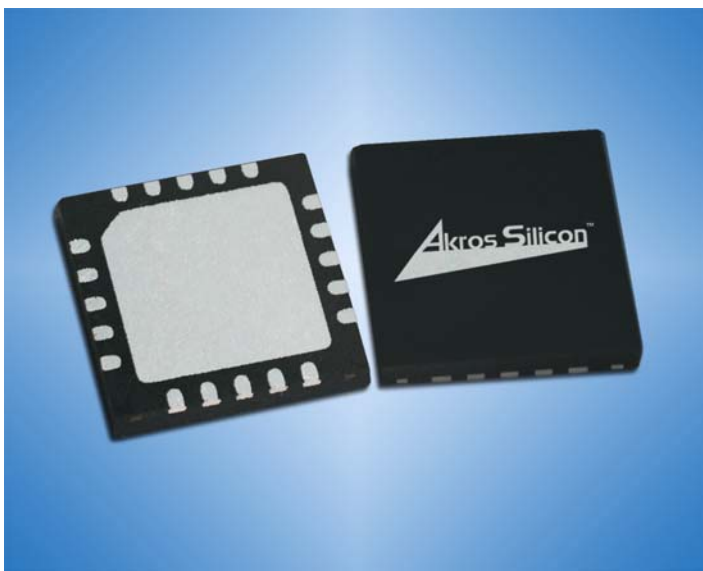


Application Note AN018

Thermal Characterization & QFN Layout Guide:

for the AS11xx Product Family

Revision 0.6, December 2007



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Introduction

The Akros AS11xx product family of PoE PD¹ controllers consists of the AS113, AS1124 and AS1130. While each device is rated for a specific power class, all devices are implemented in a 5 mm square Quad Flat-pack, No-lead (QFN) package. In the QFN, the silicon die is mounted on a copper paddle, which is part of a stamped or etched lead frame. The die and lead frame are encapsulated in plastic with conventional transfer molding methods. Rather than having leads extending from the sides, the leads are brought out as exposed pads on the bottom surface of the package. The copper paddle is also exposed, providing both a ground connection and a direct thermal path between the die and the outside surface of the package. This construction provides for a small device footprint and exceptional thermal performance.

QFN Heat-Sink

As depicted in Figure 1, most of the heat generated by the PD device is removed by conduction through the bottom surface of the package. The heat sink is essentially built into the system Printed Circuit Board (PCB). To effectively remove the heat, the PCB must provide underlying thermal pads. The PCB top layer design should include a ground paddle with thermal vias. The vias should be connected to internal ground layers and a bottom-side thermal pad. Thermal energy from the package will be drawn down the vias and away from the package. The buried ground planes and bottom thermal pad should extend beyond the dimensions of the QFN package. This will help distribute the heat energy and spread it away from the QFN package.

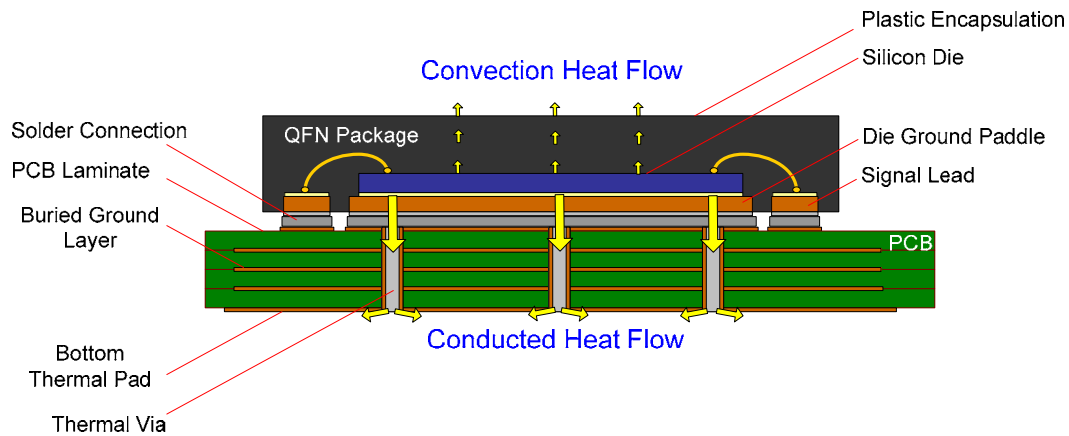


Figure 1: Cross Section of QFN package mounted on a printed circuit board

AS11xx Family PD Controllers

Akros provides the industry's smallest footprint solution for the PoE PD function. This small footprint has been accomplished by also integrating bridge diodes, protection circuitry and a DC-DC controller. Figure 2 depicts block diagrams for the Akros PD controllers. Both the AS1113 and AS1124 feature integrated bridge rectification while the higher power AS1130 solution uses external diodes.

When PoE power is applied, current flows through 2 of the diodes within the bridge rectifier. As depicted in Figures 2 and 3, each diode passes the full current delivered to the PD (I_{PORT}). For PoE Type-1 applications, the diode current can be as large as 350 mA while for Type-2 PDs, the diode current can be 720 mA. Approximately 60% of the heat dissipated in PD Controller stems from the bridge rectification diodes. Another 25% comes from the internal FET switch. The remaining logic and control circuitry consumes only 8 mA and contribute less than 20% to the chip's overall heat dissipation.

¹ Power Over Ethernet (PoE) Powered Device (PD)

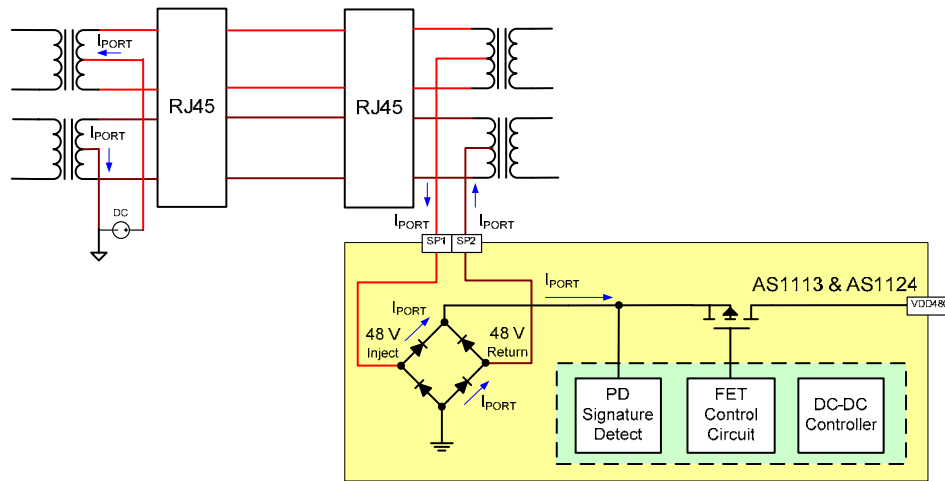


Figure 2: Block Diagrams for AS 1113 and AS1124 PD Controller with Internal Diode Bridge

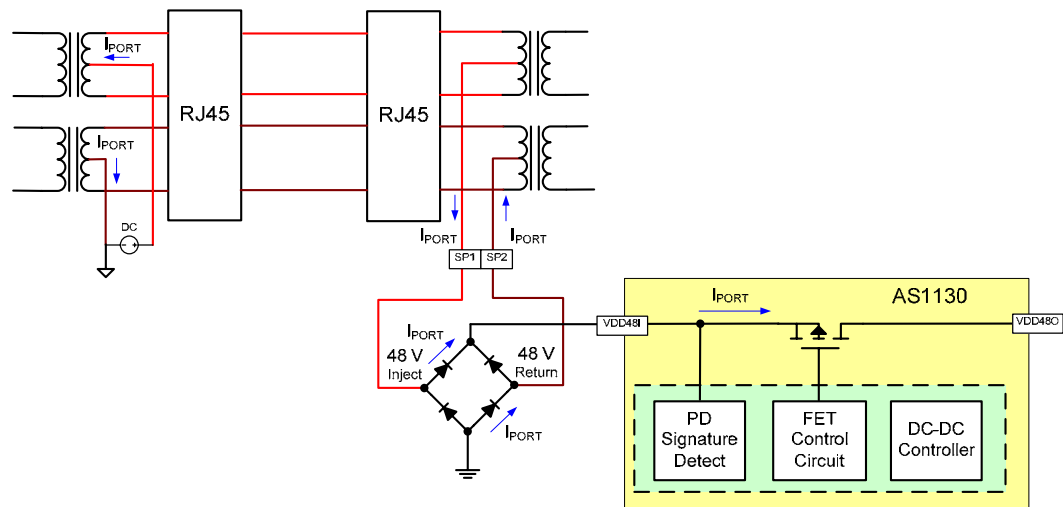


Figure 3: Block Diagrams for AS 1130 PD Controller with External Diode Bridge

Typical Power Dissipation in the AS11xx Family

Each of the Akros PD controllers has been designed for different power classes. The AS1113 was developed to address applications per the 802.3af specification. This device offers the industries smallest application footprint. However, with higher integration comes more heat generation. In comparison, The AS1130 was developed for 30W applications. This device was designed in accordance with the emerging 802.3at specification and will draw over 720 mA under full load conditions. The diode bridge is left out of the AS1130, specifically to manage the heat dissipation within the QFN package. Intermediate to the two devices is the AS1124. This device is targeted at 802.3at applications that don't require the full 30W of power, yet still need higher integration. Under full load conditions, the AS1124 can deliver up to 24W of power to the system application. However, with the integrated diode bridge the AS1124 will dissipate more heat than the AS1130, when operated under full load. The AS1124 is best applied to those intermediate applications that require power in the range between 13W and 20W. In these intermediate applications, the AS1124 heat dissipation will be comparable to the heat dissipated by the AS1130 under

full load.

To calculate the power dissipation, we have the following relation:

$$P_{DISS} = 2 * V_F * I_{PORT} + I_{PORT}^2 * R_{DSON} + V_{IN} * 8 \text{ mA}$$

Power dissipated in the bridge diodes follows a $V_F * I$ relationship, where V_F is the forward voltage drop of the bridge diodes. The power dissipated in the internal FET switch is based on an I^2R relationship while dissipation in remaining circuitry can be calculated by multiplying the bias current (8mA) by the operating voltage (48V). Table 1 summarizes the calculated power dissipation for each of the Akros PoE PD Controllers.

Table 1. Key parameters and power budget for the Akros PD Controllers

PD Device	I_{PORT} Operating Current	R_{DS_ON} Maximum FET Switch Resistance	V_F Bridge Diode Forward Voltage	P_{DIODE} Dissipation in bridge diodes	P_{FET} Dissipation in FET Switch	$P_{Control}$ Dissipation in PD and DC-DC Controller	P_{TOTAL} Total Power Dissipation within the PD Controller
AS1113	350 mA	2.0 Ω	0.9 V	0.63 W	0.24 W	0.38 W	1.25 W
AS1124	625 mA	1.5 Ω	0.9 V	0.90 W	0.37 W	0.38 W	1.65 W
AS1130	720 mA	1.5 Ω	0.9 V	1.30 W _(external)	0.78 W	0.38 W	1.16 W ¹

1. bridge diodes are external

Thermal measurements on the Akros reference designs have shows that the AS1113 and AS1130 case temperature will generally reside around 40° C under no load conditions and rise to about 52 ° C under full load. Similarly, the AS1124 will reside around 40 ° C under no load conditions and rise to about 65 ° C under full load.

Silicon Junction Temperature

If mounted properly, the QFN package and PCB board will provide enough heat dissipation to keep the silicon junction temperature under 145° C². Reliability data for the silicon process indicates that operation under this temperature limit will result in an overall failure rate of less than 21 FIT (1 failure / billion devices).

The power dissipation numbers published in the Akros datasheets have been guard-banded to represent worst case corner conditions. Table 2 identifies published power dissipation and the worst case junction temperatures. If mounted properly, the QFN package will exhibit a junction-to-ambient thermal resistance, θ_{JA} , of 31° C/W. As indicated in the table, the QFN package provides plenty of heat dissipation to maintain the silicon junction at reliable levels. The only area of caution is in operating the AS1124 at maximum power levels (24W), in which case the ambient environment should be controlled at 70° C³. If the application utilized < 20W power, then the AS1124 can be used up to industrial levels. Otherwise, the AS1130 should be used for applications that operate in +85C ambient conditions and require > 20W of power.

Also, it should be noted that the Akros PD Controller provides protection against thermal breakdown. An internal temperature monitor inside the Akros PD will begin to limit the current flowing through the internal FET, when the junction temperature reaches 145° C. If the device continues to heat-up, the FET will shut-off completely when the junction temperature reaches 160° C.

² The silicon process used by Akros is capable of reliable operation up to junction temperatures of 160 °C

³ Refer to the thermal de-rating curve in the AS1124 datasheet, pg. 15

Table 2. Worst Case Junction Temperature under Various Ambient Conditions

PD Device	P_{TOTAL} Worst Case Power Dissipation within the device	ΔT_{JA} Junction to Ambient Temperature Differential at Max Power	$T_{J25^{\circ}C}$ Junction Temperature at 25°C ambient	$T_{J70^{\circ}C}$ Junction Temperature at 70°C ambient	$T_{J85^{\circ}C}$ Junction Temperature at 85°C ambient
AS1113	1.5W	46.5 ° C	71.5 ° C	117.5 ° C	131.5 ° C
AS1124	2.4W	74.4 ° C	99.4 ° C	145 ° C	Do not use at full power
AS1130	1.7 W	52.7 ° C	77.7 ° C	122.7 ° C	137.7 ° C

Guidelines for PCB Layout

The following design guideline provides detailed design instruction for laying-out the system PCB to accept the Akros PC Controller. When laying-out the system board, the design guide should be used in conjunction with the datasheet and reference design to assure good thermal dissipation. If there are any questions or concerns, please contact Akros applications team through your sales contact or sales@akrossilicon.com

PCB Layout

As described earlier, the QFN package does not have solder balls. Electrical connection between the package and the system PCB is achieved by printing the solder paste on the system board and then reflowing the solder in a convection or infra-red (IR) oven. Reliable solder joints depend on both the PCB pad size and solder application process.

As described above, the heat sink for the QFN package is built into the system PCB. Good solder attachment is necessary for effective removal of heat generated by the PD. To achieve the desired electrical and thermal performance, the exposed thermal pad on the underside of the QFN package must be soldered to a corresponding thermal plane on the system PCB with a minimal number of voids. Care must be taken during assembly and reflow to minimize voids at the solder interface between the QFN ground paddle and PCB pad. Voids can occur due to out-gassing of solvents during the solder reflow and from solder wicking down into the thermal vias. If voids become too prominent, (>60% of the pad area), they will increase the thermal resistance of the solder interface and diminish the heat dissipation to ground pads on the system PCB. If there is a good solder interface, the thermal vias will be very effective in carrying heat away from the QFN package and distributing it to the ground planes and thermal pad on the backside of the PCB.

Figure 4 shows the dimensions for the 5mm QFN package⁴. When designing the landing pads on the system PCB, it is recommended that the PCB lead fingers be a minimum 0.10 mm longer than the package land length. The Akros QFN package has a nominal lead length of 0.40 mm. The lead pads should be designed to be at least 0.60mm long and positioned so that they also extended 0.05 mm towards the center of the package. As shown in Figure 5, the pad width should be a minimum of 0.05mm (0.025 mm per side) larger than the pad width on the QFN package. Electro-less nickel / immersion gold or electroplated nickel / gold finishes provide a good surface. Typically 5µm of nickel and 0.05 to 0.10 µm of gold are required to avoid brittle solder joints.

⁴ Based on the IPC-SM-782 is the industry standard for PCB land patterns.

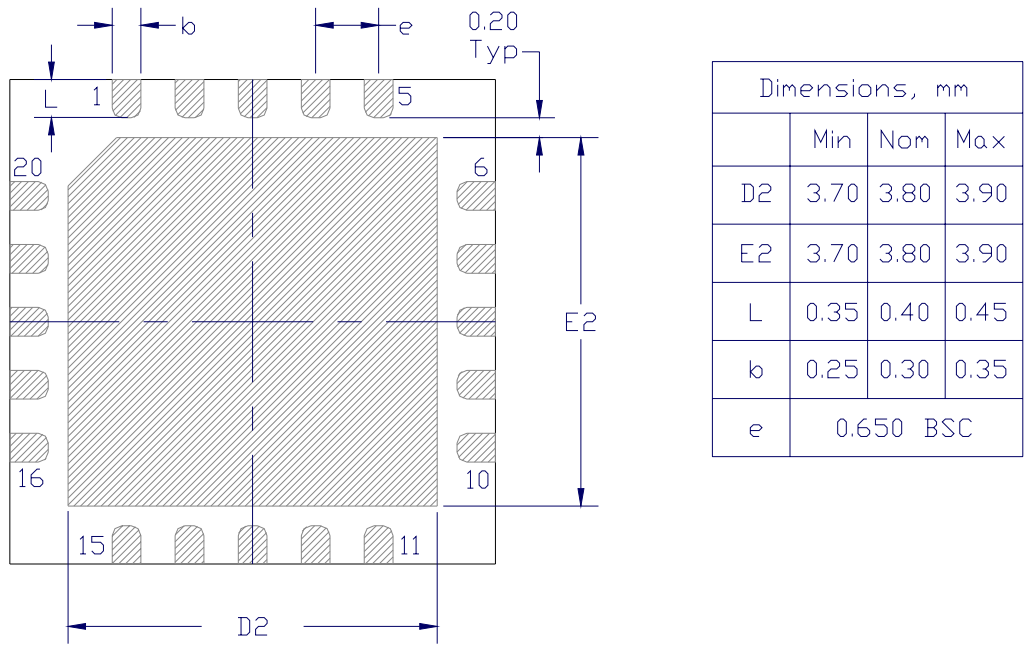


Figure 4: QFN Pad Dimensions, (viewed through the package)

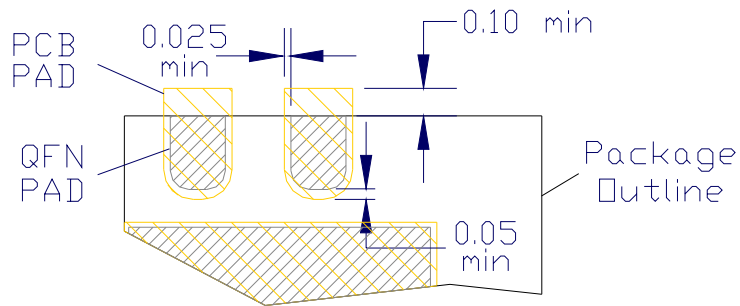


Figure 5: PCB Pad Dimensions

The number of thermal vias will determine how effectively heat is removed from the package. In the 5mm QFN package, 9 vias are practical on a 1 mm pitch. A minimum via diameter of 0.31 mm (0.012 inch) is recommended. Larger diameters, up to 0.61mm, may be used if necessary. In all cases, the barrel of the vias should be plated up to 1 oz Cu. For the 0.31 mm hole, this will effectively close the barrel to < 0.25mm.

The thermal pad of the QFN package also serves as the device electrical ground. The thermal vias should also connect to buried ground planes, within the PCB stack. On the back surface, the thermal vias should also connect to a ground pad. From the various ground pads, heat will spread through conduction and then dissipate through convection. In general, it is best to design the ground pads as large as possible to spread the heat and improve the convection process. Temperature sensitive components should be placed a minimum 0.100" (2.5mm) from the thermal pad. On the top surface of the PCB, the case temperature will run about 10 ° C cooler than the bottom pad. Most SMT chip resistors are stable enough to be placed close to the PC Controller. However, consult the manufacture's data sheet prior to laying out the PCB.

Solder Mask Design

The pads printed on the PCB can either be Solder Mask Defined (SMD) or Non Solder Mask Defined (NSMD). For the peripheral input/output pads, NSMD is recommended over SMD pads, since the copper etching process has tighter tolerance control than solder mask process. The solder mask aperture should be set-back 60 to 75 µm from the copper pads. This means that the solder mask opening be designed to be 120 to 150 µm larger than the pad size. This allows for solder mask registration tolerances, which are typically in the range of 50 µm. Using NSMD pads also improves the reliability at the solder joint. When the solder paste reflows, it is allowed to wrap around the edges of the metal pads. Figure 6 depicts the solder mask. With the 0.65 mm lead pitch, the solder mask provides approximately 0.60 mm of separation, which is sufficient to prevent bridging between lead pads. The area of greater concern is between the thermal paddle and leads. Here, it is recommended that a SMD design be used. The edge of the solder mask should be set-in to assure that there is 0.25mm of solder mask between the exposed thermal paddle and the device leads.

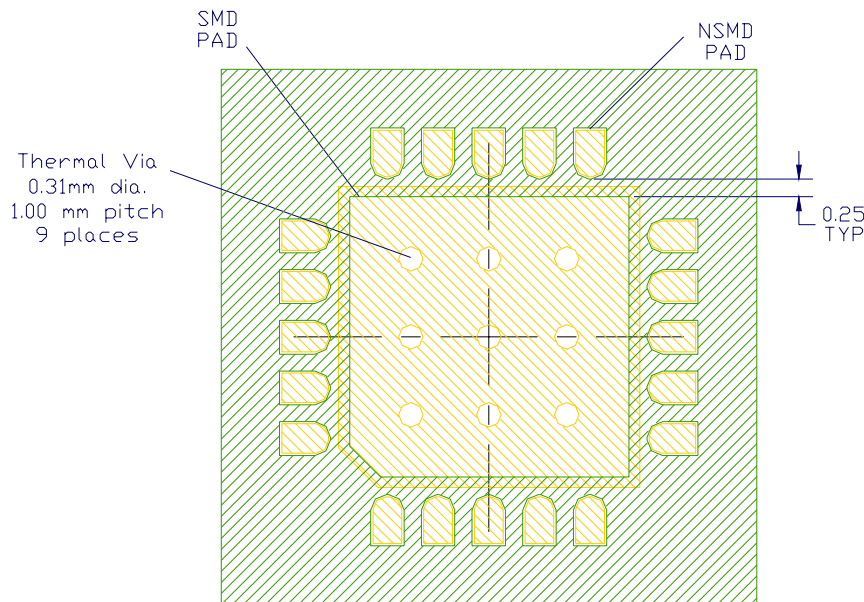


Figure 6: PCB land pattern and solder mask

Preparing Thermal Vias for Solder Reflow

During the solder reflow process, solder will tend to “wick” down the via barrels, drawing solder away from the paddle and creating voids. There are a few options to prevent this wicking effect.

- One is to plug the vias using solder or a thermally stable epoxy. Plugging the vias will provide good control over the package stand-off height. Plugged holes will also remove the opportunity for air entrapment and the solder wicking. The drawback of plugging the holes is that it adds process steps to the production flow.
- A simpler solution is to “tent” the holes by covering them with solder mask on the bottom-side of the PCB. A Liquid Photo-Image mask (LPI) is recommended. When applied some of the mask material will partially fill the hole. During IR reflow, air will out-gas from the top of the vias and counteract the capillary forces that tend to draw the solder down into the barrel of the via. The designer has the option of either covering the entire thermal pad or may either simply covering the via holes with a circular skin, often referred to as “tenting”. The tenting diameter should be 100 μm larger than the via hole diameter. For instance, a 0.41 mm pad should be used to cover a 0.31mm hole.

Stencil Design

The stencil design has much impact on the quality of the solder joints. Optimum solder joints should provide the QFN package a stand-off height of 50 to 70 μm from the system PCB. After solder reflow, inspection should show a good fillet “foot” on the input/output pads. A joint with less height, that exhibits leads without the fillet foot, indicates insufficient solder. If there is not enough solder at the interface, the part will have limited mechanical integrity under shock and vibration. If inspection shows a stand-off between the QFN package and system PC of over 70 μm , this indicated is that too much solder is applied to the joint. Another indication is solder bulging at the input/output pads, rather than a fillet foot. With too much solder, the devices are susceptible to shorts underneath the QFN package. The stencil design provides one means of controller the amount of solder applied at the interface. Often, some experimentation and visual inspection on a number of parts, is required to get the right settings.

Solder paste consists of 40% metal alloys and 60% binders, solvents and flux. During the IR reflow process, these materials boil-out of the paste and evaporate. As described above, the thermal vias can also out-gas during the IR reflow operation. If not addressed, the out-gassing of materials can cause solder bridging and voids. A common technique is to provide lanes in the solder stencil, that provide a path for out-gassing solvents.

To effectively remove this solvent and binder materials, the stencil should provide avenues for the solvents to exit. Instead of one big opening over the thermal pad area, the region should be divided into apertures. Figure 7 shows a recommended pattern for the solder stencil. The pattern will let air entrapped in 5 of the 9 vias to out-gas, before reflow occurs. The remaining four holes will out-gas through the solder paste and exit on the sides of the package.

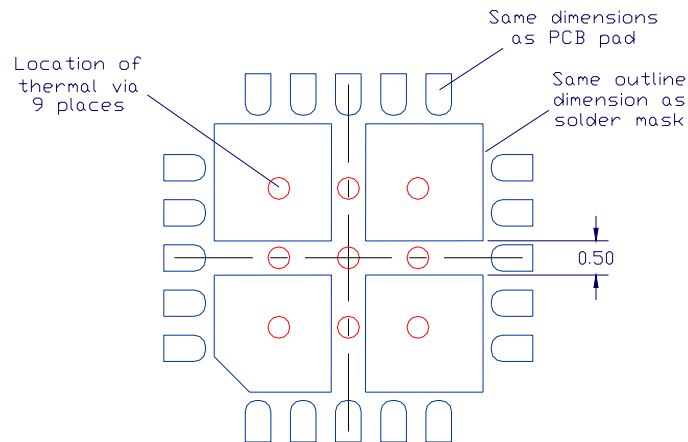


Figure 7: , recommended stencil design

A stencil this thickness of 0.15mm is recommended for the Akros QFN devices, which have a 0.65mm lead pitch. Typically the stencils are laser cut from stainless steel and should be given a slight etch to remove any burrs on the aperture walls. The etch will facilitate the pull-away from the solder. If inspection indicates that too much solder is being applied to the leads, then the pad dimensions on the stencil can be reduced by 20%, with respect to the pads imaged and etched onto the system PCB.

Solder Process

During reflow, capillary forces will cause the QFN package to naturally align with the circuit pattern on the system board. These same forces will pull the QFN package down to the system PCB. Control of the solder paste thickness is one of the most critical parameters in attaching the QFN package. If too much solder paste is used, it can actually be squeezed in between the pads and cause bridges and shorts. As indicated above, the package stand-off height is a direct function of the solder paste coverage on the thermal pad and is the best indication whether there is a good connection underneath. Cross sectioning a few of the assemblies is probably the best way to measure the stand-off on a sample basis.

Height adjustment can be achieved by refining the stencil design and screen printing operation. The solder blend, PCB finishes and reflow parameters also impact the stand-off. Some process development will be required to assure that the binder materials out-gas properly and that the bulk of the solder doesn't wick down the thermal vias. Since there is not enough space under the part for cleaning after the reflow process, it is recommended that "no clean" type 3 paste be used for mounting the QFN package. Sn63/Pb37 is commonly used. Nitrogen purge is also recommended during reflow. It is best to start with the paste manufacturers' recommended reflow profile, test the joint on multiple parts and then optimize the process settings based on the results.

Rework

The QFN parts are light enough that, if misaligned (< 50% off the part center), they will self align during reflow. Grossly misaligned part need to be removed and re-placed. As with all SMT components, it is important that the IR profiles be checked on all new board designs. The profile should be checked at different locations on the board, since the temperature may vary, depending on the mass and size of surrounding components and package densities.

Reworking QFN packages can be challenging due to their small size and the difficulty of de-soldering the large paddle. During removal, it is recommended that the board be heated from the backside pad, using a soldering iron with a blunt tip. Once the joint reflows, a vacuum pick can be used to lift-off the QFN device from the top surface.

Before replacing the part, the PCB pads must be cleaned. It is best to use a blade-style tip on the soldering iron and braided solder wick. The width of the blade should about the same width as the thermal paddle on the PCB. The soldering iron temperature should be limited so avoid damaging the printed circuit board. Once the residual solder is removed, the pads should be cleaned with a solvent, such as acetone. The solder paste manufacturer will recommend a suitable solvent.

To re-apply the device, solder paste must be applied to the PCB pads. A min-stencil & squeegee can be practical. However in most cases, the solder will need to be applied manually, while observing the part under a microscope. Some bench top re-work stations provide placement tools that will allow the QFN device to be positioned and placed with control of the X and Y and rotational axis. Once the package is placed, the solder should be reflowed with a profile similar to used in the original attachment.

CONTACT INFORMATION

Akros Silicon Inc.
6399 San Ignacio
Ave, Suite 250, sna
Jose, CA, 95119
USA

Tel: (408) 746 9000 ext. 100

Fax: (916) 351-8102

Email inquiries: marcom@akrossilicon.com

Website: www.akrossilicon.com

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