Application Note AN020

Design Guide for the AS1124-BCM5481

Revision 0.4 October 2007

Confidential

REVISION HISTORY

The revision history of the AN020 reference design document is shown in Table 1.

Table 1 AN020 Revision History

Version	Author	History Details	Date
0.1	D.Jolly	Initial release of AN020 document for review	09-04-07
0.4	J.Glick	Re-format AN020 document for review.	10-01-07

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INTRODUCTION

The development of power over Ethernet (PoE) technology has given rise to a number of applications that combine the use of the RJ45 connector as both a data port and power interface. Expanding the guidelines defined by the **IEEE®** 802.3af™ standard, the proposed **IEEE** 802.3at™ standard (PoE plus) answers demands for increased power requirements per port and flexibility for power management in such systems, especially those that support the emerging triple play media processing environment.

The AS1124-BCM5481 reference design provides an example of such a system, implementing a reduced pin count gigabit media independent interface (RGMII) that provides data stream support and incorporating a power management system.

This design guide provides details about this reference design and is intended for engineers designing PoE devices using the powered device (PD) side of the network. This design guide includes implementation details, schematics and block diagrams. For simplicity, this document refers to the AS1124-BCM5481 Reference Design as the DESIGN throughout.

MANUAL ORGANIZATION

This document uses the following sections to provide DESIGN details:

- Functional Overview — Includes a block diagram and component feature lists.
- Reference Design Implementation — Includes a functional description of each of the interface blocks.
- Reference Design Schematics
- Design Layout — Includes considerations for layer assignments, signal trace design, and general circuit board layout.

DEFINITIONS

Definitions for terms used in this document are defined below for reference. Terms and acronyms are listed in this section for reference.

AN020	Application Note xxx
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharged
IEC	International Engineering Consortium
IEEE	Institute of Electrical and Electronics Engineers
PD	Powered Device

PRODUCT FEATURES

The DESIGN provides proven technology with low-cost components that support rapid development of PoE Ethernet applications to support emerging market requirements. It offers an optimal solution that balances clock frequency and pin count for the data transmission in the Ethernet interface and provides an efficient and low-cost solution for providing a regulated and low-EMI power system for PoE PDs. Because the devices do not require special thermal handling or heat-sinks, the DESIGN minimizes required board space and height. The DESIGN also represents a competitive advantage in reducing time-to-market in developing applications quickly.

FEATURES

The DESIGN uses the following components:

- BCM5481 integrated triple-speed Ethernet transceiver
- AS1124 Powered Device (PD) Controller with integrated DC-DC Controller

APPLICATION BLOCK DIAGRAM

The AS1124-BCM5481 reference design implements an RGMII interface from the 1GBE PHY to the MAC Interface on the host interface. The application block diagram is shown below in Figure 1 for reference.

DESIGN BLOCK DIAGRAM

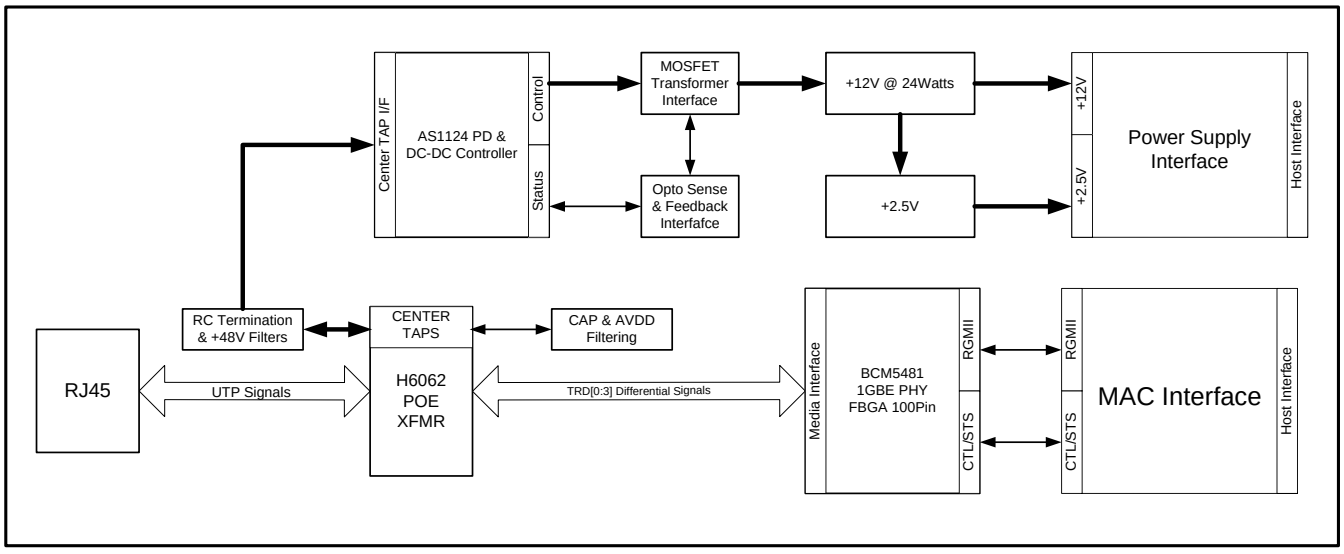


Figure 1 DESIGN Block Diagram

FUNCTIONAL OVERVIEW

The DESIGN provides the required subsystems to implement a fully compliant PoE gigabit Ethernet PHY design. Akros Silicon devices are designed to comply with the **IEEE** 802.3af standard to supply power and data used by a 10/100/1000 triple speed Ethernet device. The following sections provide a list of features for the BCM5481 gigabit Ethernet PHY Device and AS1124 PoE devices.

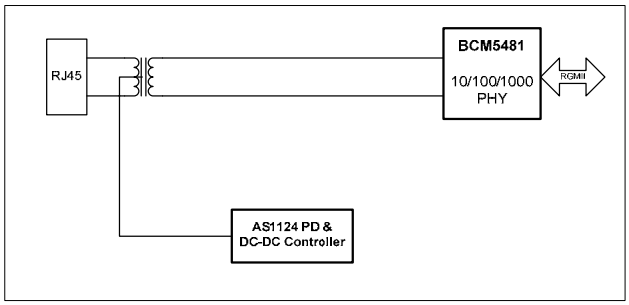


Figure 2 AS1124-BCM5481 Block Diagram

BCM5481 Features

- Single-Chip integrated triple-speed Ethernet transceiver – MAC to Magnetics:
  - 1000Base-T **IEEE** Std. 802.3ab
  - 100Base-T **IEEE** Std. 802.3u
  - 10Base-T **IEEE** 802.3® standard
- GMII, RGMII and MII MAC interface options.
- Ethernet @ WireSpeed™
- Integrated voltage regulators
- Trace matched output impedance
- Lineside loopback
- Low electromagnetic interference (EMI) emissions
- Cable plant diagnostics
- Robust cable sourced electrostatic discharged (CESD) tolerance
- Support for jumbo packets up to 10 KB
- Detection and correction of pair swaps (MDI crossover), pair skew, and pair polarity
- Advanced power management
- **IEEE** Std. 1149.1™ (JTAG) boundary scan
- Super isolate mode
- 9 x 9 mm, 100-pin FBGA Package

AS1124 Features

- Fully supports **IEEE** Std. 802.3af-2003 and supports pre-standard **IEEE** Std. 802.3at-2006™ power requirements.
- Meets IEC 61000-4-2/3/4/5/6 requirements.
- Meets IEC 60950 over-voltage protection requirements.
- Integrated rectification for superior high voltage protection.
- Integrated DC-DC converter, provides exceptional EMI performance.
- Programmable DC current limit up to 800 mA.
- Supports “two finger” classification for the proposed standard **IEEE** Std. 802.3at-2006 higher power PD applications.
- Provides seamless support for local power.
- Over-temperature protection.
- 5x5 mm, 20 lead QFN Package, RoHS compliant.

REFERENCE DESIGN IMPLEMENTATION

BCM5481 IMPLEMENTATION

The BCM5481 consists of a triple-speed 1000Base-T/100Base-TX/10Base-T Gigabit Ethernet transceiver integrated into a single monolithic CMOS chip. The device performs all physical-layer functions for 1000Base-T, 100Base-T, and 10Base-T Ethernet on standard category 5 unshielded twisted pair (UTP) cable. 10Base-T can also run on standard category 3, 4, and 5 UTP. The BCM5481 is a highly integrated solution combining digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders, decoders, echo cancellers, crosstalk cancellers, and all required support circuitry. Based on Broadcom's proven Digital Signal Processor (DSP) technology, the BCM5481 is designed to be fully compliant with GMII, RGMII, and MII specifications, allowing compatibility with industry-standard Ethernet MACs and switch controllers.

Designed for reliable operation over worst-case category 5 cable, the BCM5481 automatically negotiates with its link partner to determine the highest possible operating speed. The device detects and corrects most common wiring problems. The BCM5481 features CableChecker™ Diagnostics, which detects common cable problems including shorts, opens, and cable length.

The DESIGN implements the RGMII functionality. While any of the interface modes could be used, this mode provides a balance that uses half the clock frequency of the SGMII (lower EMI generation) and fewer signal lines/pins than the MII implementation.

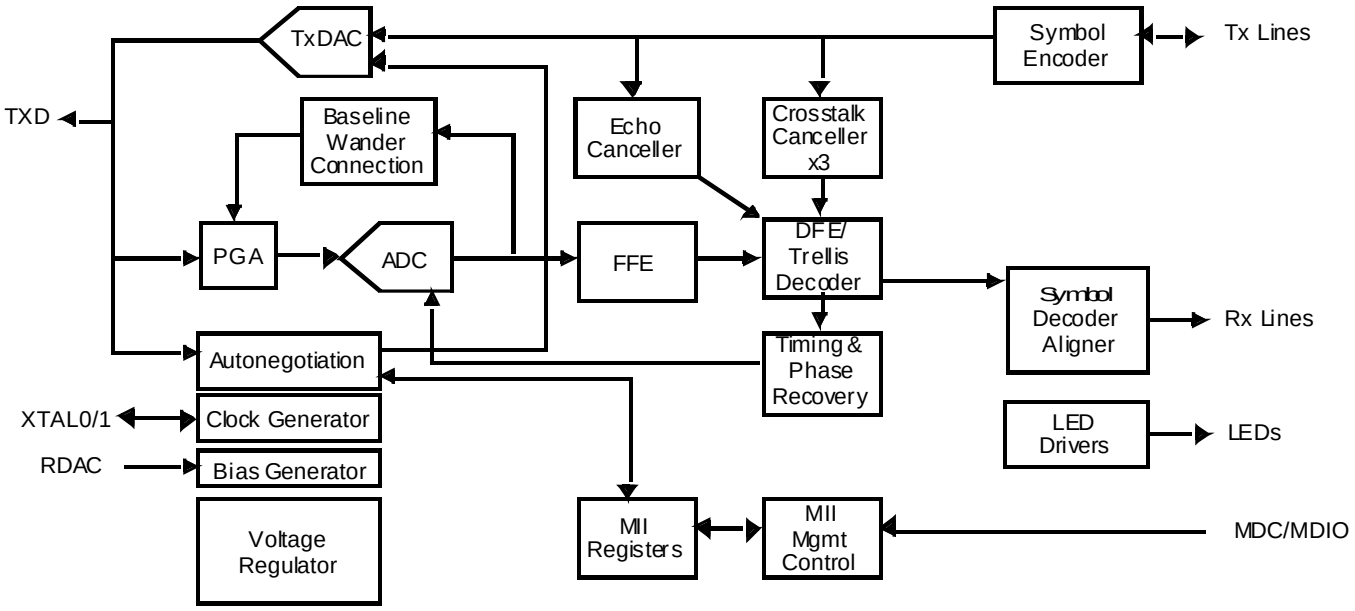


Figure 3 BCM 5481 Block Diagram

AS1124 IMPLEMENTATION

The AS1124 is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE). Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security and Web Cameras, Analog Telephone Adapters (ATA) and Point of Sales Terminals. The AS1124 provides the functions required for power over Ethernet Powered Device (PD) applications.

The AS1124 integrates rectification and protection circuitry, a PD controller, and a DC-DC converter. This high level of integration provides faster response to surge events and limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device. The device is designed to provide a safe low impedance discharge paths directly back to the earth ground, resulting in superior reliability and circuit protection.

AS1124 has been designed to address both EMI emission concerns and surge/over-voltage protection in POE applications. The AS1124 design minimizes transmission of system common-mode noise on to the UTP while providing high immunity to over-voltage and surge events. The DESIGN uses a single AS1124.

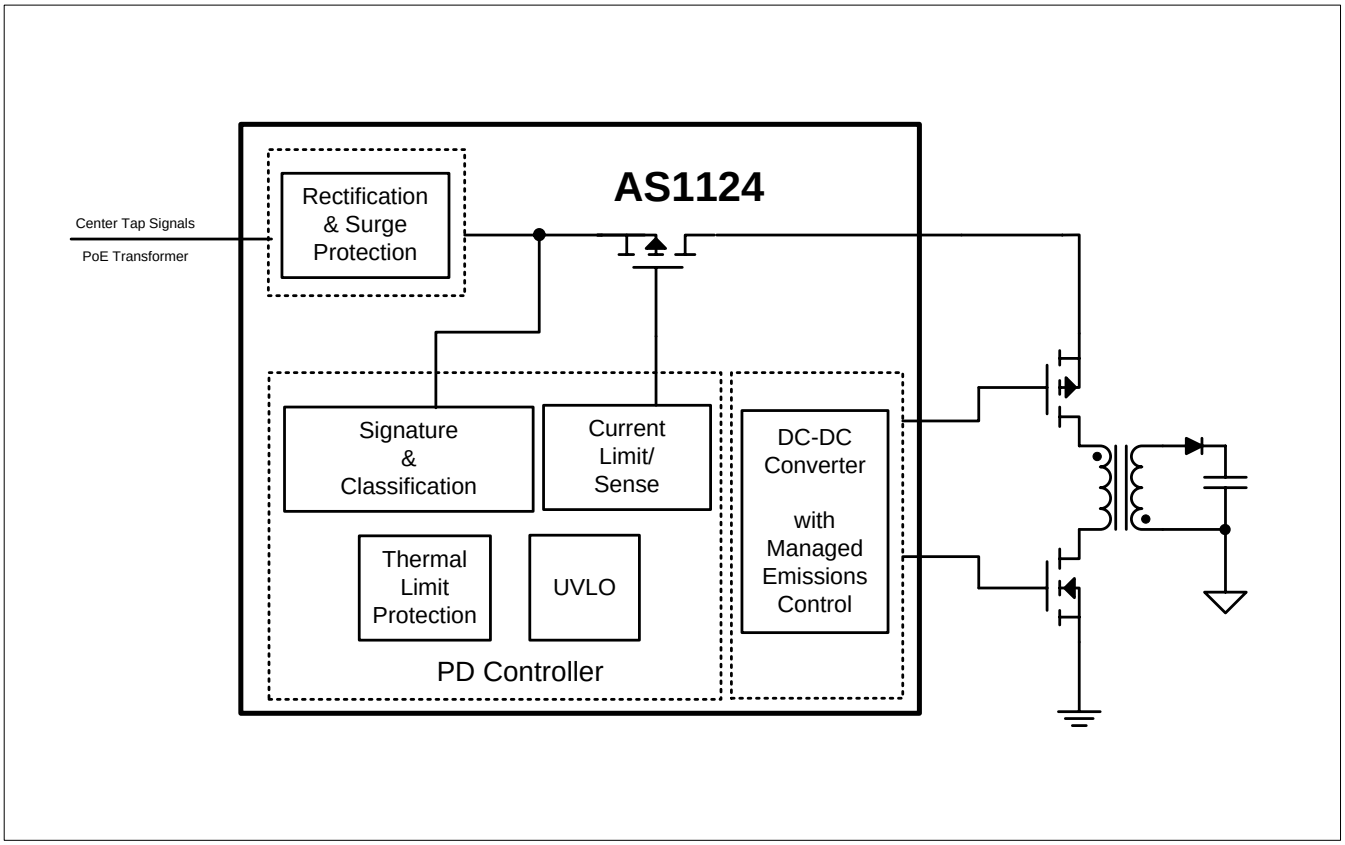


Figure 4 AS1124 Block Diagram

REFERENCE DESIGN SCHEMATICS

The schematics show the implement details for the three major components and supporting circuitry: BCM5481 1GBE PHY device and the AS1124 PoE device.

BCM5481 SCHEMATICS

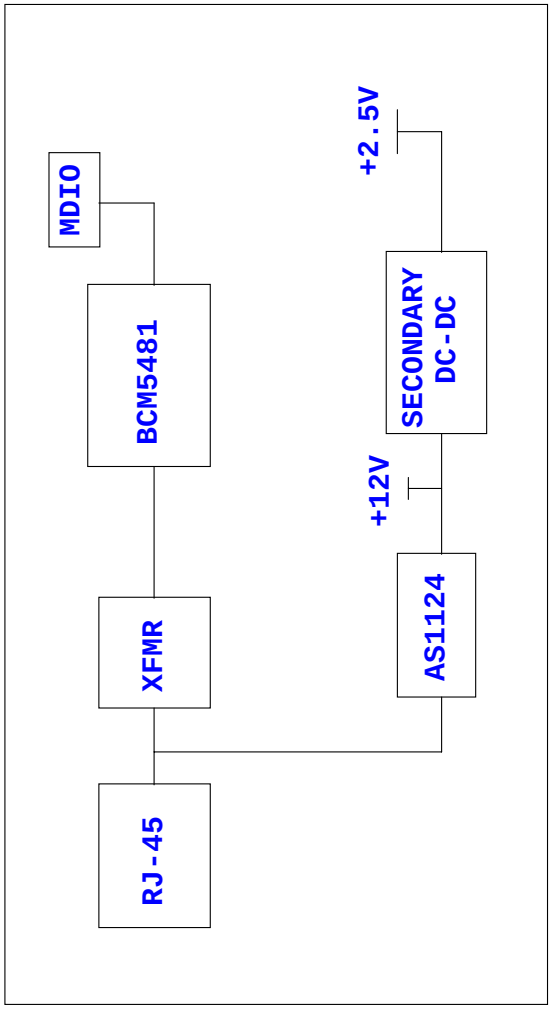
The BCM5481 1GBE PHY is located on Sheet 4 of the schematics. The TRD [0:3] signal pairs interface from the PoE 1GBE Transformer. The RGMII Signals interface directly to the 1GBE MAC interface. The voltage interface is shown on Sheet 5 of the schematics.

AS1124 SCHEMATICS

The AS1124 DC-DC Converter Interface is located on Sheet 3 of the schematics. The PoE 1GBE Transformer center tap signals provide the DC voltage source signal to the AS1124 device. The remaining circuitry for the DC-DC converter is shown on Sheet 3 for reference.

Platform	Date	Schematic Revision	Schematic Changes and/or Updates
AS1124-BCM5481 RD, PCB Rev A	06-28-07	REV A	Schematics updated for AS1124-BCM5481 Reference Design.
AS1124-BCM5481 RD, PCB Rev A	07-10-07	REV A	Initial Release of Schematics for AS1124-BCM5481 Reference Design.
AS1124-BCM5481 RD, PCB Rev A	09-26-07	REV A	Removed AS1602 device from Schematics, AS1124-BCM5481 Reference Design.

AS1124- BCM5481 Reference Design



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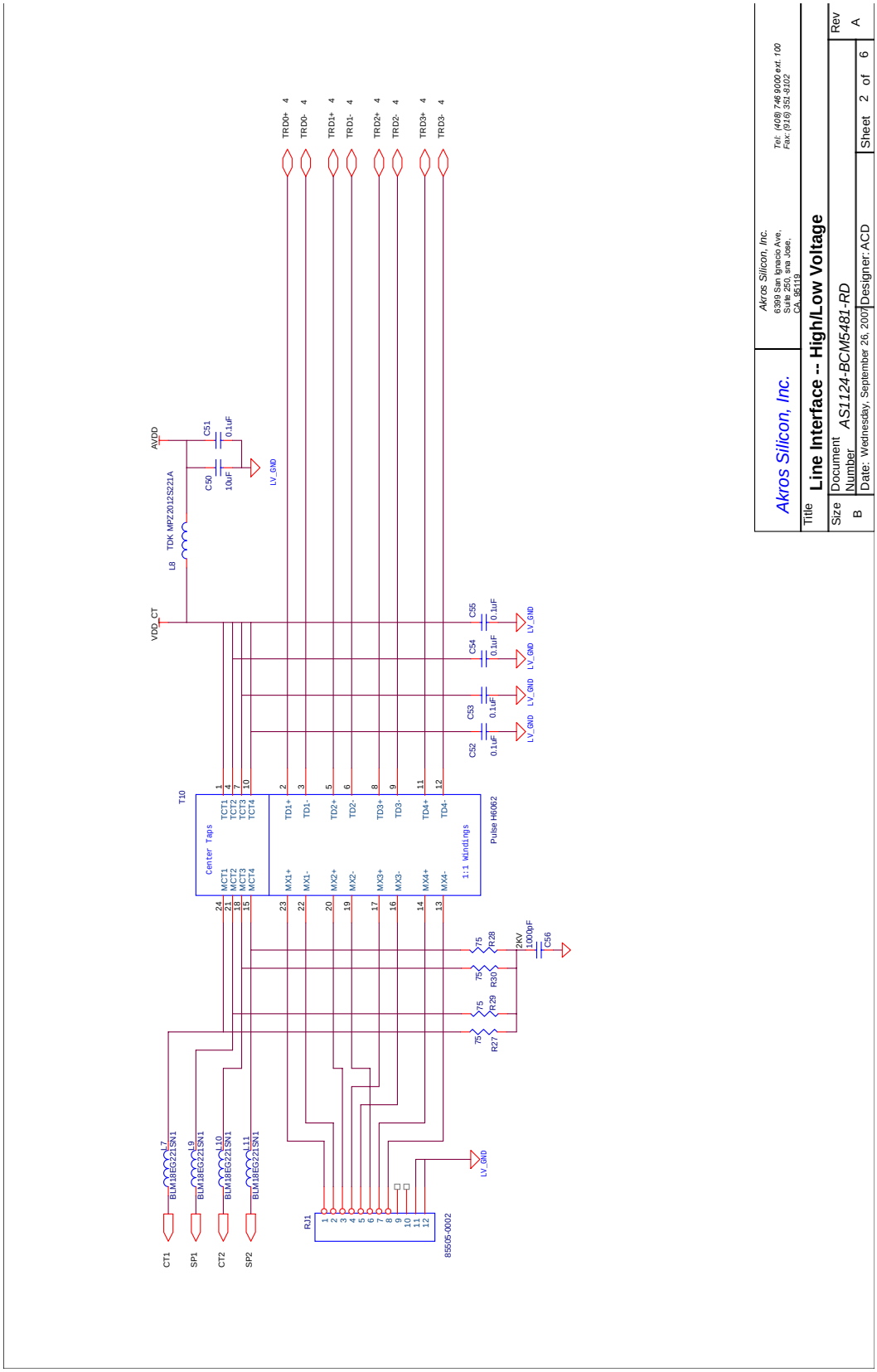
Title: AS1124-BCM5481 Reference Design

Size: B | Document Number: AS1124-BCM5481-RD | Rev: A

Date: Wednesday, September 26, 2007 | Designer: ACD | Sheet 1 of 6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Title
Line Interface -- High/Low Voltage
Size
B
Document Number
AS1124-BCM5481-RD
Rev
A
Date: Wednesday, September 26, 2007
Designer: ACD
Sheet 2 of 6
AVDD
VDD_CT
TDK MPZ2012S221A
L8
C51 0.1uF
C50 10uF
LV_GND
TRD0+ 4
TRD0- 4
TRD1+ 4
TRD1- 4
TRD2+ 4
TRD2- 4
TRD3+ 4
TRD3- 4
C55 0.1uF
C54 0.1uF
C53 0.1uF
C52 0.1uF
T10
Center Taps
MCT1
MCT2
MCT3
MCT4
TCT1
TCT2
TCT3
TCT4
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
TD4+
TD4-
MX1+
MX1-
MX2+
MX2-
MX3+
MX3-
MX4+
MX4-
1:1 Windings
Pulse H6062
75 R28
75 R30
75 R29
75 R27
2KV 1000pF C56
L7 BLM18EG221SN1
L9 BLM18EG221SN1
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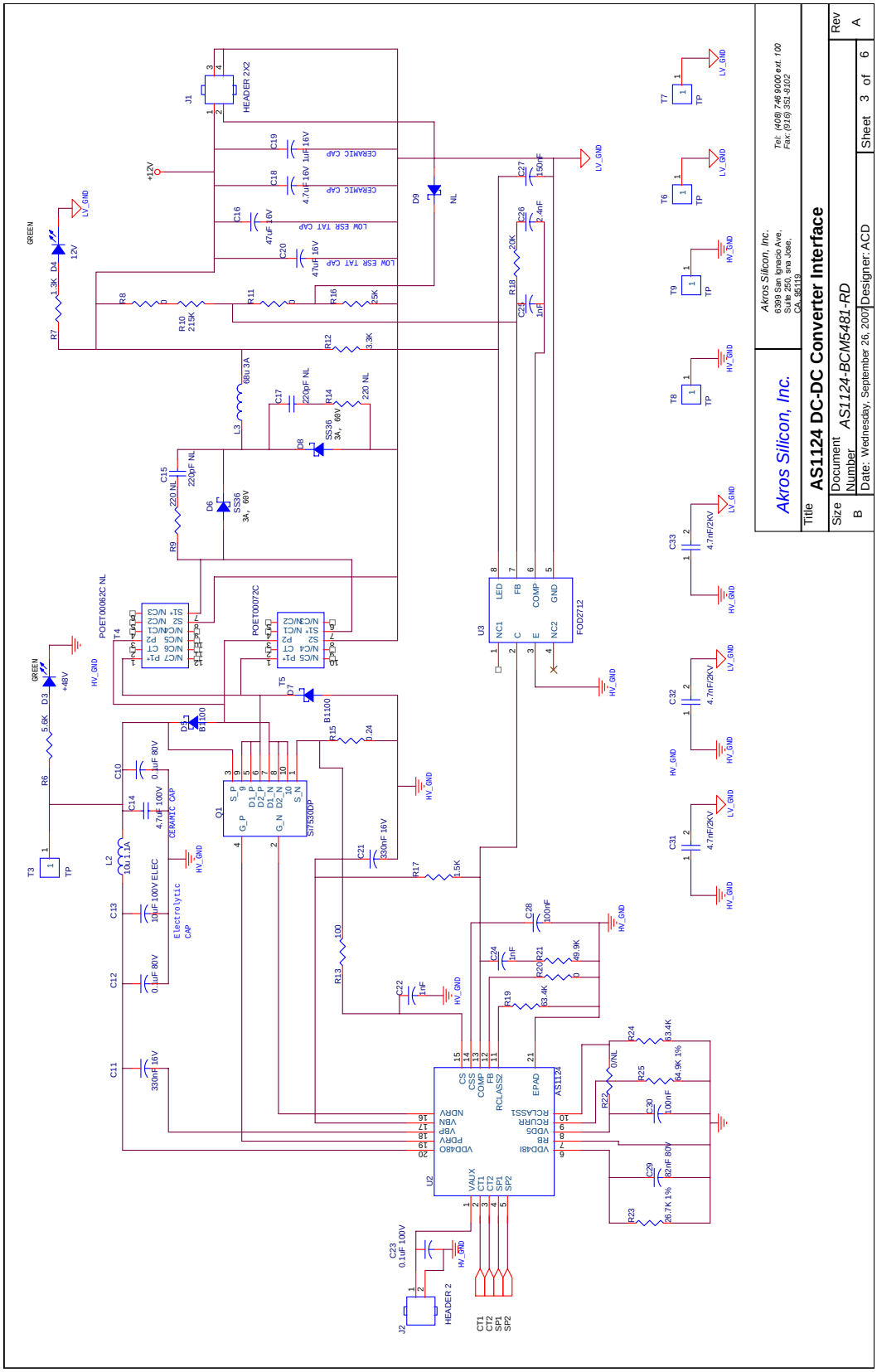
CT1
SP1
CT2
SP2
RJ1
85505-0002


Akros Silicon, Inc.
AS1124 DC-DC Converter Interface
Document Number AS1124-BCM5481-RD
Rev A
Size B
Sheet 3 of 6
Date: Wednesday, September 26, 2007
Designer: ACD
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6390 San Ignacio Ave, Suite 200, San Jose, CA 95119
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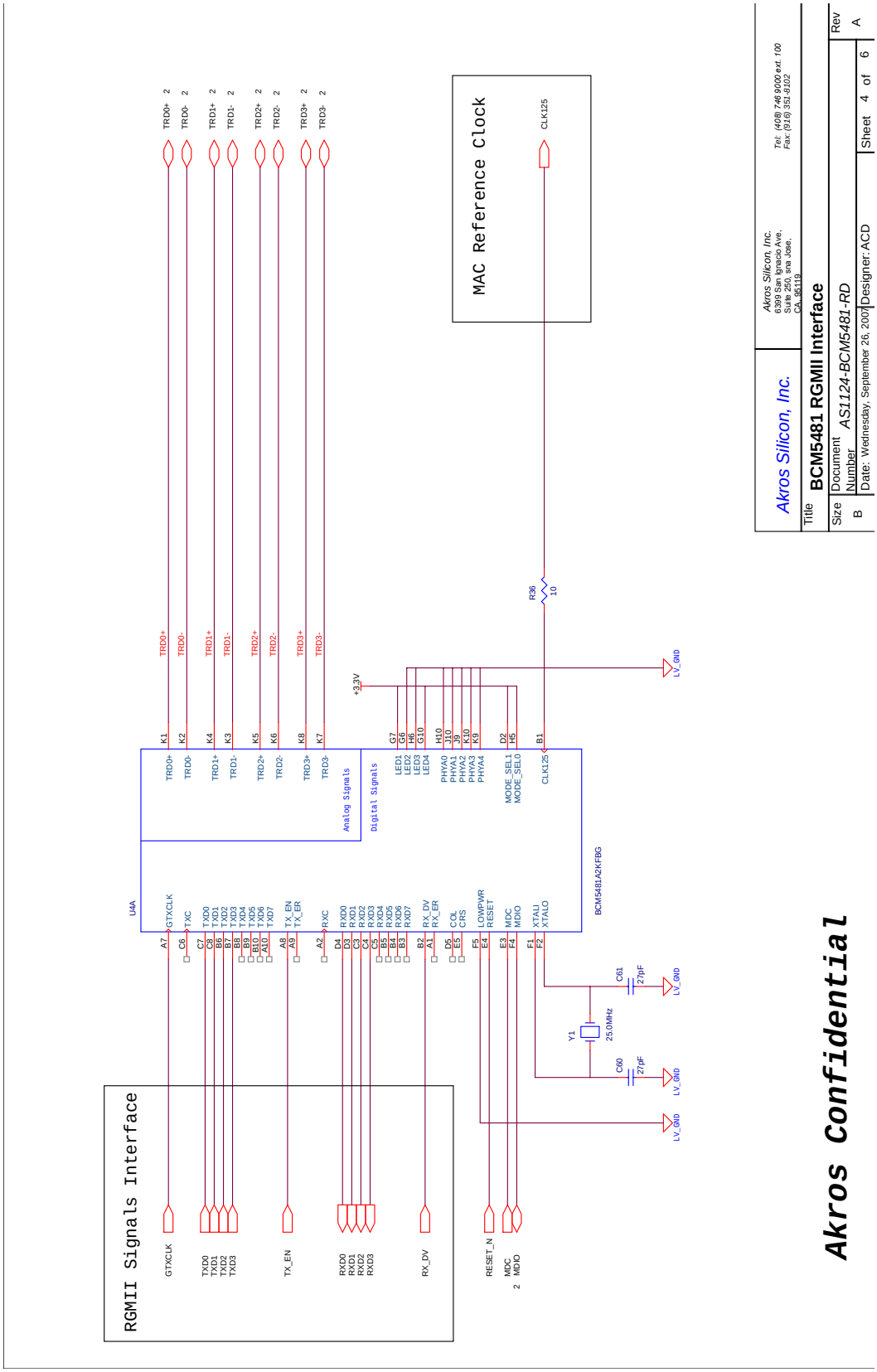
Fax: (916) 451-8102
HEADER 2X2
HEADER 2
AS1124
FOD2712
STS30DP
POET00062C NL
POET00072C
SS36
3A, 60V
B1100
CERAMIC CAP
LOW ESR TAT CAP
Electrolytic CAP
CERAMIC CAP
TP
LV_GND
HV_GND
+12V
+48V
GREEN
NL


RGMII Signals Interface
MAC Reference Clock
BCM5481A2KFBG
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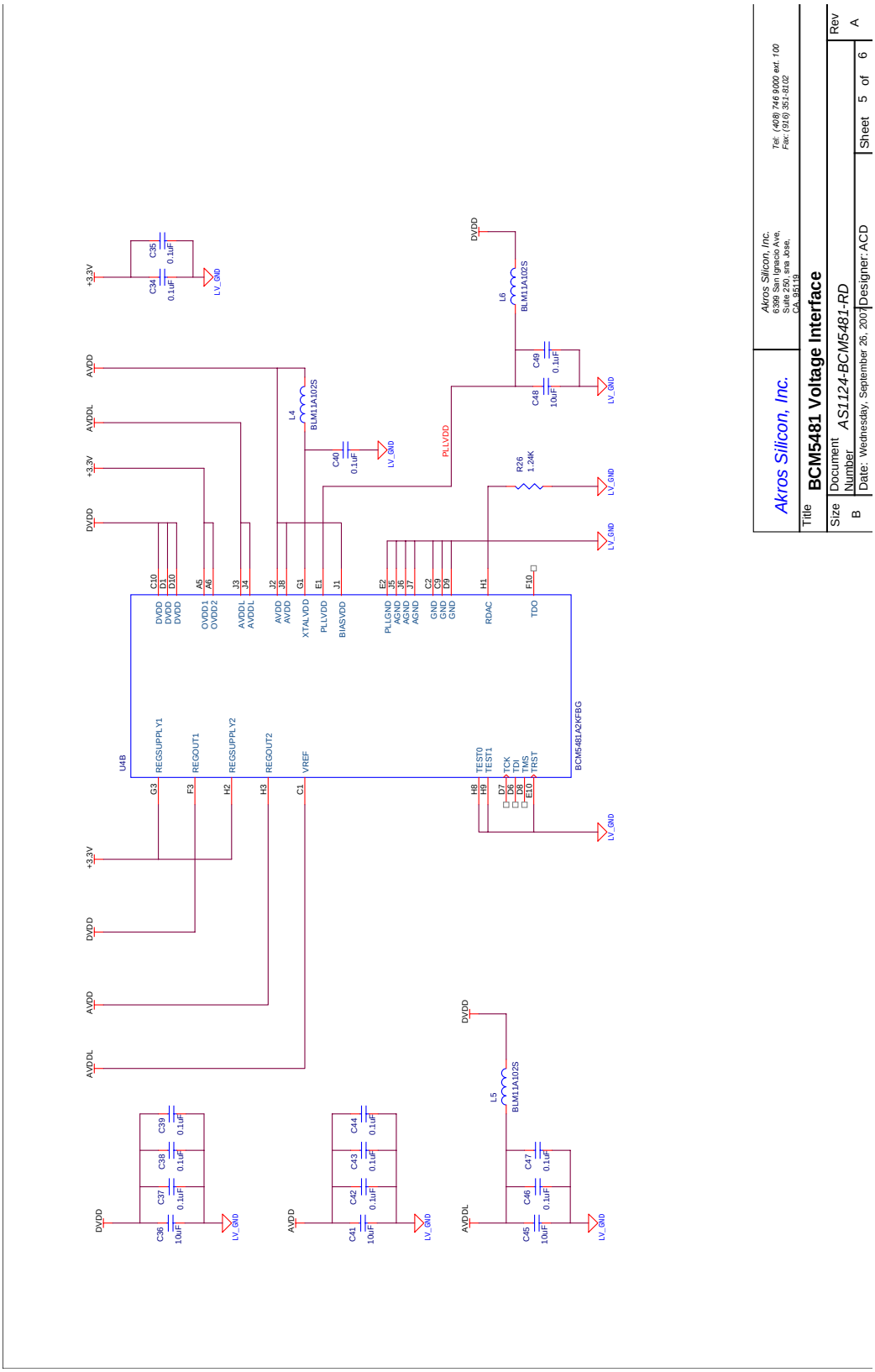
BCM5481 RGMII Interface
AS1124-BCM5481-RD
Date: Wednesday, September 26, 2007
Designer: ACD
Sheet 4 of 6
Rev A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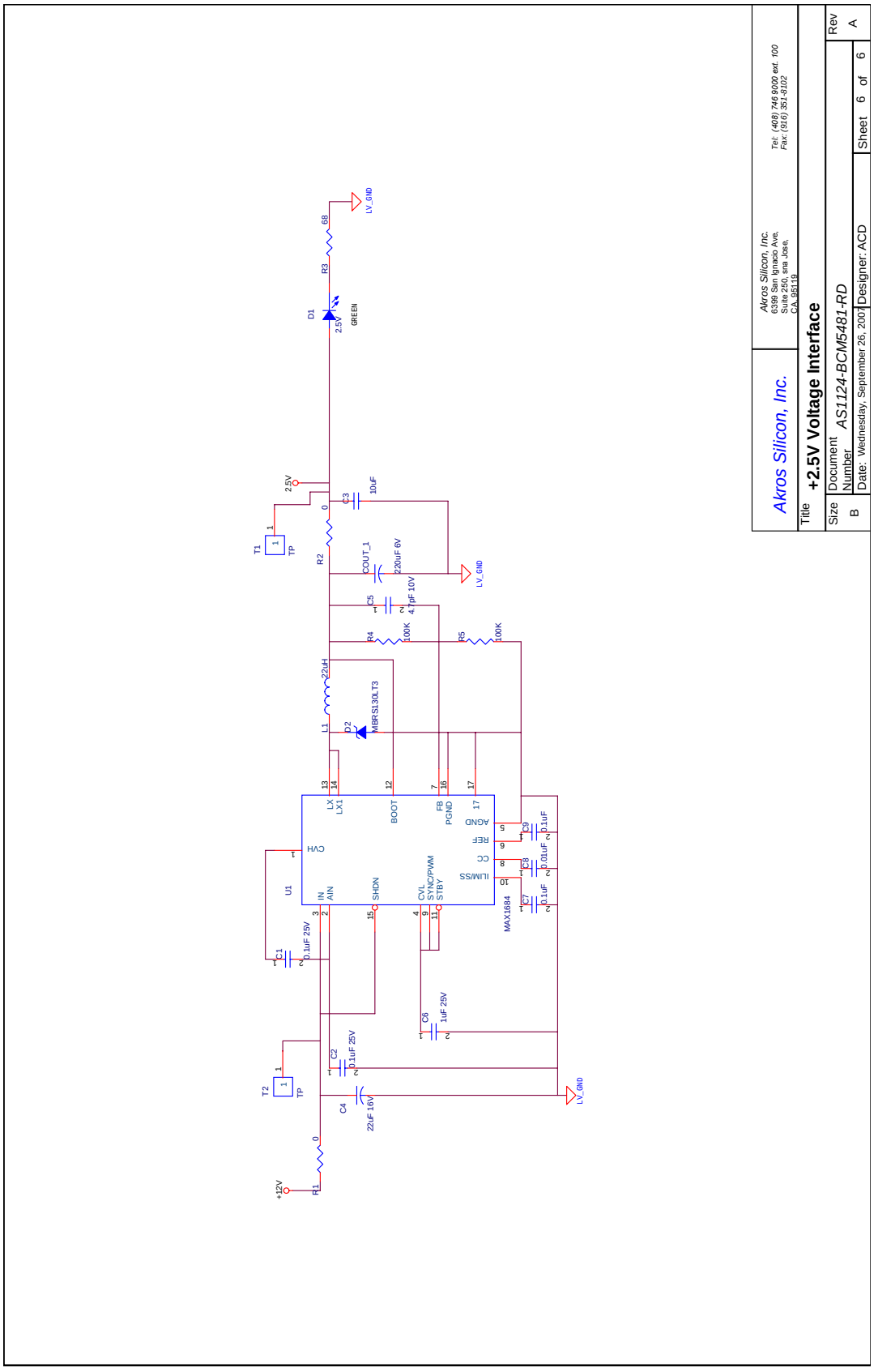
Title BCM5481 Voltage Interface
Size B
Document Number AS1124-BCM5481-RD
Rev A
Date: Wednesday, September 26, 2007
Designer: ACD
Sheet 5 of 6
U4B
BCM5481A2KFBG
REGSUPPLY1
REGOUT1
REGSUPPLY2
REGOUT2
VREF
TEST0
TEST1
TCK
TDI
TMS
TRST
RDAC
TDO
XTALVDD
PLLVDD
BIASVDD
PLLGND
L4
L5
L6
BLM11A102S
R26
1.24K
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
0.1uF
10uF
+3.3V
DVDD
AVDD
AVDDL
PLLVDD
LV_GND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Title
+2.5V Voltage Interface
Size
B
Document Number
AS1124-BCM5481-RD
Rev
A
Date: Wednesday, September 26, 2007
Designer: ACD
Sheet 6 of 6
LV_GND
68
R3
D1
2.5V
GREEN
2.5V
10uF
C3
T1
TP
R2
COUT_1
220uF 6V
4.7pF 10V
C5
100K
R4
100K
R5
22uH
L1
D2
MBRS130LT3
LX
LX1
BOOT
FB
PGND
AGND
REF
CC
ILIM/SS
CVH
IN
AIN
SHDN
CVL
SYNC/PWM
STBY
U1
MAX1684
0.1uF
C9
0.01uF
C8
0.1uF
C7
0.1uF 25V
C1
1uF 25V
C6
0.1uF 25V
C2
T2
TP
22uF 16V
C4
0
R1
+12V

DESIGN LAYOUT

The PCB layer assignments provide details on PCB Layers, signal routing layers, Ground planes and Power/Ground planes. Impedance information for Differential signal routing and Single-end signal routing is required for PCB Layout.

The PCB Fabrication Vendor provides this detailed information for the PCB Layout. The following information was provided by Merix (www.merix.com) for the 6 Layer PCB Stack-up.

Layers	Signal Type
Layer 1	Signal Routing (Top)
Layer 2	Ground Plane
Layer 3	Internal Signal Routing
Layer 4	Power/Ground Planes
Layer 5	Ground Plane
Layer 6	Signal Routing (Bottom)

LAYER ASSIGNMENTS

The PCB Layer Assignments are recommended for a 6 layer PCB design. Below is the recommended PCB Layer Assignment for copper thickness, copper weight, and layer thickness for each PCB layer as shown in Figure 6. The PCB Layers is assigned as follows:

The PCB stack-up supports Differential Routing at 100 Ohms and Single-Ended Routing at 50 Ohms. The Differential Routing is required for UTP Signals and TRD Signals from the RJ45, to/from the PoE transformer and to/from the 10/100/1000 Ethernet device.

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	2.00	0.5 oz			Foil, 0.5 oz
			4.00	4.80	Prepreg IS410 2116
2	1.20	1 oz			
			4.00	4.00	Core IS410 4mils 1-2116 1 oz / 1 oz 18x24
3	1.20	1 oz			
			4.00	3.30	Prepreg IS410 2113
			4.00	28.00	Core IS410 28mils 4-7628 0.5 oz / 0.5 oz 18x24
			4.00	3.30	Prepreg IS410 2113
4	1.20	1 oz			
			4.00	4.00	Core IS410 4mils 1-2116 1 oz / 1 oz 18x24
5	1.20	1 oz			
			4.00	4.80	Prepreg IS410 2116
6	2.00	0.5 oz			Foil, 0.5 oz

Layers	Drill Type	Via Fill		
1 - 6	PTH	--	57.00	Thickness over Laminate
			61.00	Thickness over Copper
			62.40	Thickness over Soldermask

Figure 5 PCB Layer Assignments

The Single-Ended routing is used for high speed clock and digital signals at 50 Ohms.

The Impedance Table for the 6 Layer PCB stack-up is shown in Table 2 for reference. The Differential Routing for external layers (Layers 1 & 6) and internal layers (Layers 3 & 4) have different trace widths and line pitch. The bulk of the Differential Routing will be on external layers, depending on the complexity of the design some routing will be on internal layers.

Table 2 Impedance Table – 6 Layers PCB Stack-up

Impedance Table										
Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Edge Coupled Pitch * (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)	CoPlaner Space (mils)
1	Single Ended	Yes	50.00	+/-5	8.00	--	(2)	8.00	49.32	
1	Edge Coupled Differential	Yes	100.00	+/-10	4.50	10.00	(2)	4.50	101.31	
3	Edge Coupled Differential	---	100.00	+/-10	4.00	12.00	(2, 4)	4.25	99.20	
4	Edge Coupled Differential	---	100.00	+/-10	4.00	12.00	(3, 5)	4.25	99.20	
6	Single Ended	Yes	50.00	+/-5	8.00	--	(5)	8.00	49.32	
6	Edge Coupled Differential	Yes	100.00	+/-10	4.50	10.00	(5)	4.50	101.31	

SUMMARY

The AS1124-BCM5481 reference design implements an RGMII that incorporates a power management system for PoE PDs. The design employs devices to minimize signal noise that can corrupt transmitted data and to meet regulatory EMI requirements. By using low-power, small footprint devices that do not require special heatsinks or other thermal protection, the DESIGN can be used as a reference to enable quick development of applications such as Voice over IP (VoIP) phones, wireless LAN access points, security and web cameras, Analog Telephone Adapters (ATA), and Point of Sales Terminals.

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Website: www.akrossilicon.com

REFERENCES

This section lists any outside references that contain information not included in this document that may aid in understanding this document. Refer to the appropriate document for additional information.

- AS1124 24W, Powered Device with integrated DC-DC Controller, Akros Silicon, Datasheet Revision 1.1, May 2007.
- Design Guide for AS1113/AS1124 PoE Powered Devices, Akros Silicon, Application Note AN004 Revision 0.7 May 2007.
- BCM5481 10/100/1000BASE-T Gigabit Ethernet Transceiver, Broadcom, 5481-DS08-R 05/14/07.

IMPORTANT NOTICES

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