
**Application Note AN083**

# AS1834/54 Assembly Guide

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***Preliminary Release***

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## ABOUT APPLICATION NOTE AN083

Application Note AN083 describes recommended design best-practices for board-level PCB assembly of the Akros AS1854 series products. These include AS1824, AS1834, AS1844 and AS1854. Included are guidelines for how to assemble boards with the 0.4mm-pitch QFN package and how to optimize the signal pad and thermal pad design.

Refer to www.akrossilicon.com for further details on these and other Akros Silicon components. For any further assistance, please contact your Akros sales representation or contact us at support@akrossilicon.com.

## ASSEMBLY CONSIDERATIONS FOR QFN PACKAGES

The quad flat no-lead package provides the advantages of near chip scale package size with very efficient thermal performance. By using the die attach pad of the package as the primary ground path and the direct path of thermal conduction and soldering the entire pad directly to the printed circuit board (PCB), the electrical and thermal resistance of the package to the PCB is drastically reduced. Care must be taken to ensure the thermal path at the PCB interface can properly distribute the heat from the package into the bulk of the board.

Other considerations in the PCB design and assembly with regard to these packages involve PCB finish, pad design, solder mask coverage, vias types, solder paste coverage of the signal pads and thermal pads, stencil design, solder joint quality, thermal profiling, and solder past type. This paper is intended to provide guidelines on these issues. This is only a guideline to help the designer in developing a proper PCB design and assembly process for this QFN package. Further evaluation and development effort may be required to maximize the PCB design and assembly for the user's practices and requirements.

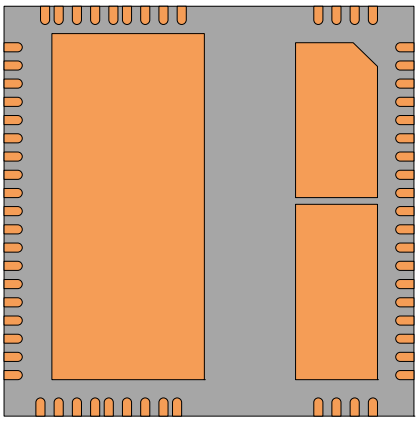
For reference, the following items reflect the best known recipe to date for assembly of the AS1854 onto Akros' validation boards:

- Stencil thickness – 4 mils
- Type4 solder with no clean flux - solder paste used is Alpha Metals No Clean OM350 (particle 4)
- Signal pads designed with 15 mils toe distance, pad width set to 8 mils
- NSMD for thermal pads

## PCB FOOTPRINT

This package uses a single row of perimeter pads (signal pads) and three independent thermal pads. The signal pads on this package are rectangular with a radiused end near the thermal pads. The three thermal pads provide three different return current paths for the device. The two smaller thermal pads on the primary side provide return current paths for V48N and V48RTN as well as a thermal path for the primary side of the input converter. The third thermal pad provides ground for the secondary side and a thermal path for the secondary converters. The primary-side thermal pads and the secondary thermal pad need to maintain the same separation as the thermal pads on the package to ensure protection from dielectric breakdown of air between the pads in the event of a large voltage difference between the primary and secondary return voltages.

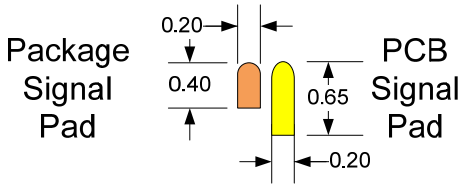
**Figure 1 - As viewed from bottom of the package**



## SIGNAL PAD DESIGN

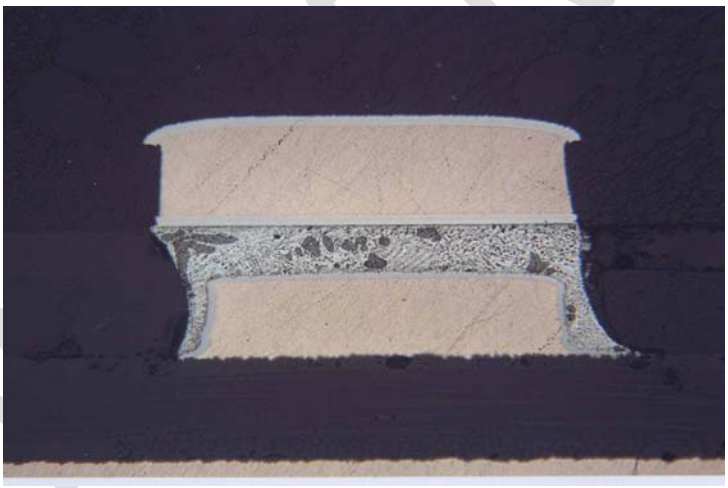
The signal pads on the PCB should match the width and location of the corresponding pads on the package and should be elongated away from the center of the package by at least 0.05mm (from IPS toe fillet recommendations).

**Figure 2 - Package and Signal Pads**



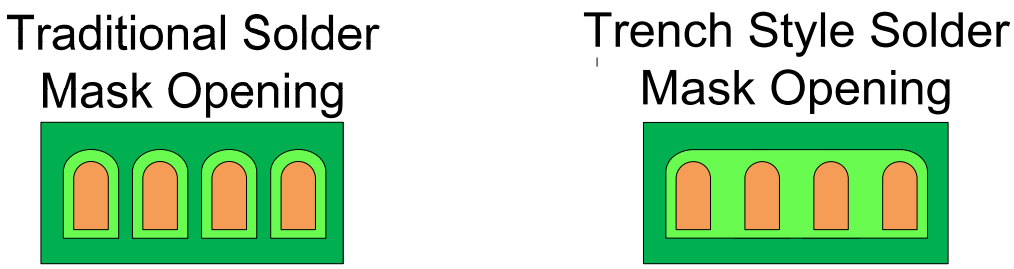

The signal pads should be NSMD (non-solder mask defined), since the metal tolerance on PCB fabrication is much tighter than the tolerance of the solder mask. Also with the NSMD pads the solder will wrap around the edge of the signal pad providing an improved solder joint.

**Figure 3 - Solder Wrapping Around Edges of Pads**



The opening of the solder mask for the pads should be 120-150um larger than the pads. Since most PCB manufacturers need 75um of solder mask webbing between pads to provide proper adhesion and also require 50-65um of registration tolerance, there is insufficient space between signal pads on this package to produce reliable solder mask webs between pads. Therefore the recommendation is to use “Trench” type solder mask openings around the signal pads. It is recommended that the inner edge of the solder mask opening be radiused to ensure adequate solder mask webbing between adjacent signal rows in the corners.

**Figure 4 - Solder Mask Openings**

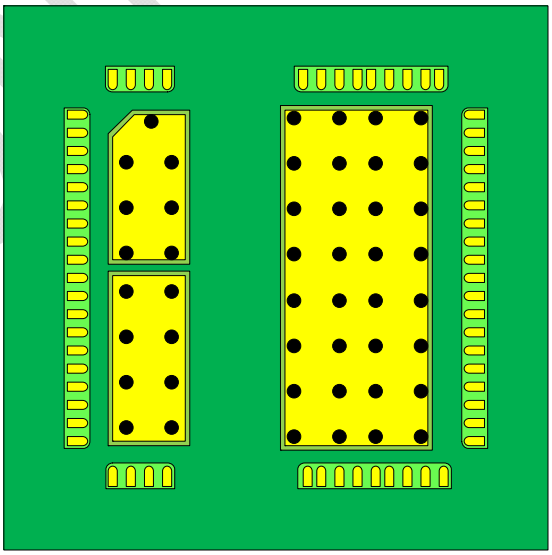



## THERMAL PAD DESIGN

The size of the thermal pad on the PCB should match the size of the thermal pads on the package. Due to the minimal spacing between the signal pads and the thermal pads, the thermal pads should be SMD (solder mask defined) to avoid the risk of solder bridging. The solder mask should overlap the thermal pad by 100um on all 4 sides, providing a minimum 25um solder mask overlap under all conditions.

The thermal pads in the center of the package require the use of thermal vias as defined in the JEDEC standard. Thermal vias should be 300um (12mil) finished diameter with a minimum of 33um (1.3mil) metal plating and be spaced on 1.00-1.20mm centers. The design of the thermal vias and stencil needs to consider two issues with regard to the thermal pads: voiding and standoff height of the package. To a major extent, the standoff height of the package is determined by the volume of solder on the thermal pad. This can be affected by voiding above the thermal pad and wicking of solder into vias during reflow. Generally voiding does not significantly degrade the thermal performance or thermal transfer from the package into the PCB. In fact, up to 50% voiding has not shown significant degradation in simulation. An exception, however, is if the size of the voids approaches the spacing of the thermal vias. In this case, single vias may become ineffective because the void increases the thermal resistance path beyond the distance to the next available via.

**Figure 5 - PCB Footprint**



## BOARD FINISH

The board finish should be OSP, Silver Immersion, or Gold Plating. HASL does not provide a flat enough surface and may lead to open signal(s) and/or poorly controlled stand-off height of the package.

## SOLDER PASTE

Due to the target standoff height of 50-75um, there is insufficient space between the package and board to allow effective cleaning of the flux after reflow. Therefore, it is recommended that “No Clean” paste be used for mounting this package. Nitrogen purge is also recommended during reflow to reduce oxidation during reflow.

## STENCIL DESIGN

The optimum solder joints on the perimeter pads should have about 50 to 75 microns (2 to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirements. The first step in achieving good standoff is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

$$AspectRatio, A_1 = \frac{ApertureWidth}{StencilThickness} = \frac{W}{T}$$

$$AreaRatio, A_2 = \frac{A_{PAD}}{A_{WALL}} = \frac{L \times W}{2T \times (L + W)}$$

$$A_{PAD} = L \times W$$

$$A_{WALL} = 2T \times (L + W)$$

For reliable solder past transfer from the stencil to the PCB, the Aspect Ratio should be maintained at least 1.5 and the Area Ratio should be at least 0.66. (IPC-7525, “Stencil Design Guidelines”, IPC, Northbrook, IL, May 2000)

$$TransferEfficiency; TE = 2.404 \times (AreaRatio)^{3.426}$$

(From Alpha Metals)

**Table 1 - Stencil Thickness and Apertures**

| Stencil Thickness | Aperture Width | Aperture Length | Aspect Ratio | Area Ratio | Transfer Efficiency |
|---|---|---|---|---|---|
| 100 | 200 | 650 | 2.00 | 0.765 | 0.96 |
| 100 | 180 | 650 | 1.80 | 0.705 | 0.73 |
| 125 | 200 | 650 | 1.60 | 0.612 | 0.45 |
| 125 | 180 | 650 | 1.44 | 0.564 | 0.34 |

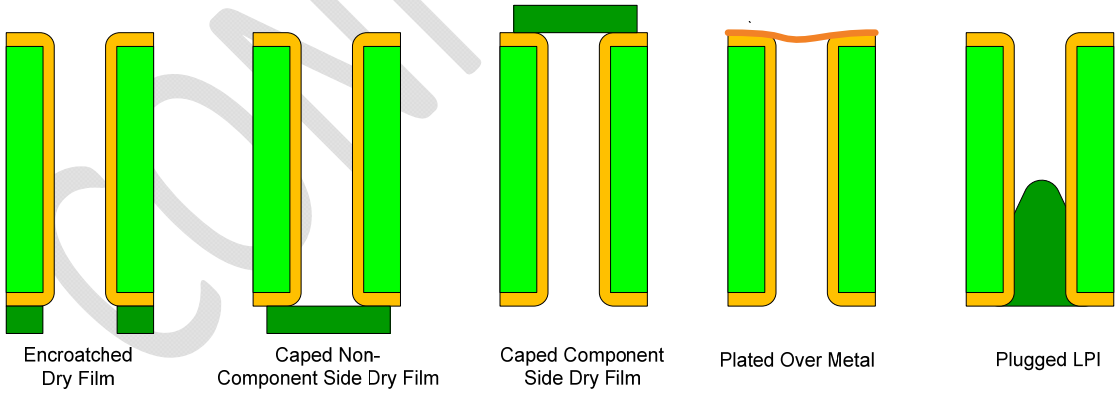
Standard stencil thickness ranges from 100-150um (4-6 mil) for laser-cut stencils with tapered apertures. For the aperture sizes required to match the signal pad of this footprint and to maintain a reliable paste transfer, either a 125um (5 mil) stencil with signal pad openings equal in width to the PCB pad should be used, or a 100um (4 mil) stencil, if narrower openings are desired. To minimize the risk of solder bridging from the signal pads to the thermal pads, the stencil opening may be offset away from the thermal pad (~20um); all signal pads are 400um center to center.

Since the standoff height is essentially defined by the volume of solder remaining between the thermal pad on the package and on the PCB, to minimize the variation of this volume, care should be taken to minimize voids and avoid having solder wick down the thermal via in the pad. Avoiding voids requires there be sufficient escape access for the flux in the paste, this can be accomplished by venting out through the open thermal vias or by applying the past to the thermal pads in a regular pattern allowing the flux to vent off before the solder becomes liquidus.

Again the open vias pose a problem with controlling the volume of solder remaining between the package and the PCB. This may be controlled by encroaching the via on the far side of the PCB. The other approach of applying the solder paste in a pattern allows the vias to be closed, thus avoiding the wicking issue all together, but care must be taken to ensure the volume of solder present on the thermal pad will provide 50-75um of stand-off. Typical solder pastes have 40-60% solid metal by volume, and usually the pattern apertures for the thermal pad are sufficiently large that essentially 100% of the solder transfers to the PCB during screening. The closing of the vias may have issues depending on the method employed.

Vias that are plated shut generally have some dimpling and may not be possible at all foundries for vias of this diameter. Capped or plugged vias from the opposite side of the board may result in trapped air in the via that will expand rapidly during reflow and may lead to greater voiding. Capping the vias from the top may cause significant surface protrusion during solder screening. In some cases the best solution is a combination of patterning, with a combination of closed and/or encroached vias. To achieve optimal results for a given PCB fabricator and assembly shop will require some experimentation.

**Figure 6 - Via Cross Sections**



# REFLOW SOLDERING GUIDELINE FOR SURFACE MOUNT DEVICES

## REFLOW PROCESS

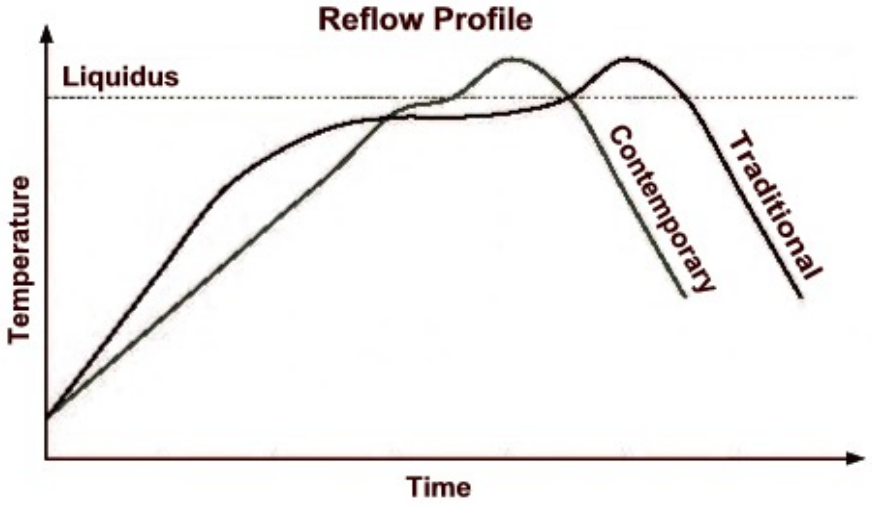
In surface mount assembly, a key step is reflowing deposited solder paste to form the solder joints. Each solder paste formula has a temperature profile that produces quality solder joints with minimum defects. To achieve the desired soldering results, every solder joint on the board needs to be heated similarly. Many factors, including the furnace, the PCBs, and the components on the board influence the temperature of the printed solder paste. Therefore each board design has an individual optimal reflow temperature profile that is dependent on its material properties, available equipment, and solder paste.

The soldering process can be thought of as having the following phases:

- Solvents are driven from the solder paste as the board is heated up
- The flux is activated to clean the solder balls and the surfaces to be soldered
- The solder paste melts to form a compound at the interface
- The board is cooled to solidify the molten solder.

Two typical solder profiles are shown below:

**Figure 7 - Solder Profiles**




The traditional profile had a long “soak” time. The reason for this was the use of infrared reflow ovens. These types of ovens caused the components on the board to have large differences in temperature. To minimize the large differences in temperature it is necessary to have a long soak period to equalize the temperature on the PCB before going into the reflow zone. With modern convection ovens, the large differences in temperature are largely eliminated, and a long soak time is not necessary.

The first step in the profile is to heat the assembly from room temperature to a temperature that evaporates the solvents from the solder paste. This is often referred to as the “preheat stage”. The second step in the process is to bring the assembly up to a temperature at which the flux in the paste turns from a solid to a liquid and becomes active. In order for the flux to do its job well, it must remain

within a temperature window for a certain period of time. This is referred to as "soak time." Caution must be taken not to extend the soak time too long or achieve too high of a temperature or the flux can be used up prematurely. The third step in the process is to melt the solder. The final step is to cool the assembly to room temperature.

## REFLOW OPTIMIZATION

New PCB's should always be characterized to a specific reflow. Improper reflow temperature may cause manufacturing defects and even damage the components on the board. The following discussion provides some guidance on how to minimize various manufacturing defects caused by poor reflow temperature profile.

## PREHEAT STAGE

Prior to reflow, the solder must be heated to drive out the solvent. As the solder paste is heated, its viscosity drops. This is caused by thermal agitation at the molecular level. The decrease in viscosity will cause the solder to spread out or slump. There is however, a counter reaction due to solvent evaporation. As the solvents evaporate, the viscosity of the material will increase. In ramping up the temperature, our goal is to eliminate or minimize solder slump due to potential bridging of the solder. This can be achieved by balancing the two processes involved. Thermal agitation is purely temperature dependent, while solvent evaporation is both temperature and time dependent. With a controlled temperature increase, the loss of viscosity due to thermal agitation will be counteracted by the increase in viscosity due to solvent loss.

Slump is the direct cause of many reflow-related defects, such as solder bridging and beading. Solder slump causes the solder paste to spread out under the component. During reflow, small solder balls may break from the main body of solder as it melts and tries to pull up into a single bead. Solder beading may also be caused by excessive solvent evaporation during the preheat stage. If this out-gassing force overcomes the cohesive force in the paste, isolated aggregates of paste are forced out under the component. During reflow, these isolated islands of paste melt and coalesce into balls at the side of the component.

With the traditional profile, there is a danger that the fast ramp-up rate may cause solder slump and/or eruption of the solder paste. If a traditional profile is required, care should be taken to use as slow a ramp-up rate as possible to reduce the likelihood of bridging, solder beading and solder balling caused by solder slump and explosive out-gassing.

However, care should be taken not to use too slow a ramp rate. The trend to low residue paste means there is less rosin in the paste. This rosin acts as a protective barrier against oxidation. Large convection ovens tend to have very high airflow, which tends to oxidize the solder powder in the paste. The lower rosin content reduces the protective barrier against oxidation.

## SOAK

Fluxes contain organic acids or esters of acids that degrade with time and temperature. Most fluxes activate at around 145ºC and quickly begin to break down above 150ºC. If this temperature is not reached during the soak period only partial cleaning of the solder pads are performed and wetting problems can occur. On the other hand if the soak time is to long, the flux has used up all its cleaning potential before the reflow zone is reached and wetting of the joint can be compromised.

Therefore, keeping the preheat profile cool will preserve the life of the activator longer. After reaching 150 the peak temperature should be reached as quickly as possible. Flux reaction usually takes place very quickly. Long soak time compromises the life of the activator of the paste, thus promoting opens at the solder joints.

## REFLOW

During the reflow process the solder powder melts, coalesces and forms an intermetallic layer between the solder and the circuit board, and the solder and the component. Time and temperature above liquidus during the reflow process is a critical factor in ensuring a properly soldered assembly.

Generally, the solder is superheated above its melting point to allow the solder to coalesce. The goal of the dwell time is to achieve optimal solder spread on solder joints across the circuit board while reducing flux entrapment and voiding. The appropriate dwell time depends on the degree of population and mass of the PCB. If the population and mass of the PCB are light, the dwell time can be shorter than for a heavily populated and high-mass PCB. If the dwell time is too short, it will result in poor wetting of the solder pad due to lack of time for the solder alloy to wet the entire solder pad. The typical time above liquidus is 30 to 90s. This ensures that the entire assembly receives sufficient superheat to solder properly.

On the other hand if the dwell time is too long, say more than 120 seconds, the intermetallic layer in the solder joint will grow thicker which may compromise the reliability of the solder joint.

In addition to time above liquidus, the peak temperature reached during the soldering process is also vital. For example, when soldering a copper substrate with Sn63/Pb37, the peak temperature is generally in the range of 205° to 215°C. Too high of a reflow peak temperature can lead to excessive copper dissolution and intermetallic formation and damage. Flux damage can occur if certain temperatures are exceeded during the reflow process. Organic acids or esters of acids begin to decompose around 150°C. Some other organic acids such as rosin are active up into the mid-200°C range. As the decomposition of these materials begins, their soldering ability rapidly degrades. Excessive heating may also cause solder to wick up into undesired areas on components and PCBs that are undesirable.

## COOLING

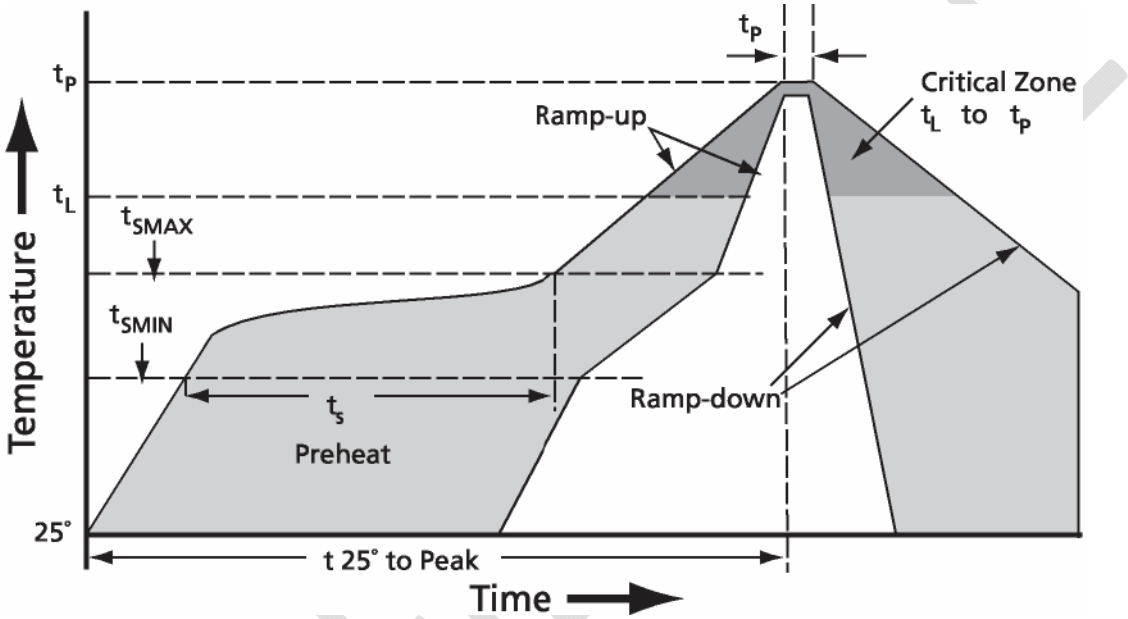
The cooling phase is an equally important phase to the other three phases. The importance of the cooling is often underestimated but the strength of the finished solder joint depends on the speed of cooling. For the solder joint to form a strong bond between the solder pad and the component terminal, the cooling should be as fast as possible. Despite appearances, tin and lead do not mix in the solder joint. When cooling rapidly, the tin and lead areas in the solder joint are smaller, resulting in a larger bonding surface between the two.

A slow cool down will also result in an excessive intermetallic layer growth and makes the joint hard but brittle. However, the maximum temperature decrease gradient is set by the strengths of the components. The components simply crack if the temperature drops too rapidly. The cooling should therefore be 3-4 degree Celsius per second down to around 130 degree Celsius. Below 130 degree Celsius the cooling rate is not important to the solder joint quality and can be less.

## REFLOW PROFILE GUIDELINE FOR COMPONENTS

Although component suppliers cannot provide a specific profile for each of their components, the Joint Electron Device Engineering Council (JEDEC) has developed guidelines for reflow processes. These guidelines provide limits to ensure the robustness of components and provide a basis for our customers to develop a reflow profile to attach components successfully. These profiles are used to classify the components based on their robustness to absorbed moisture. All devices provided by Akros Silicon, Inc. are compliant to JEDEC J-STD-020. Figure 8 below depicts the allowable window for the reflow of surface mounted devices.

**Figure 8 - Classification Reflow Profile**




The specific parameter values are given in the following tables. Note all temperatures refer to the top side of the package, measured on the package body surface. The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients, due to differences in the thermal mass of SMD packages, may still exist. The package volume excludes external terminals (balls, bumps, lands, leads) and/or non-integral heat sinks.

**Table 2 - Classification Reflow Profiles**

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| Average Ramp-Up Rate ($Ts_{max}$ to Tp) | 3°C/second max. | 3°C/second max. |
| Preheat<br>Temperature Min ($Ts_{min}$)<br>Temperature Max ($Ts_{max}$)<br>Time ($Ts_{min}$ to $Ts_{max}$) | <br>100°C<br>150°C<br>60-120 seconds | <br>150°C<br>200°C<br>60-180 seconds |
| Time maintained above:<br>Temperature ($T_L$)<br>Time ($t_L$) | <br>183°C<br>60-150 seconds | <br>217°C<br>60-150 seconds |
| Peak/Classification Temperature (Tp) | See Table 2 | See Table 3 |
| Time within 5°C of Actual Peak Temperature (tp) | 10-30 seconds | 20-40 seconds |
| Ramp-Down Rate | 6°C/second max. | 6°C/second max. |
| Time 25°C to Peak Temperature | 6 minutes max. | 8 minutes max. |

## REWORK

### COMPONENT REMOVAL

The first step in component removal is the reflow of solder joints attaching the component to the board. Ideally the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquidus can be reduced as long as the reflow is complete. In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters, and hot gas or air should be used on the top side of the component. Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided since this may cause QFN to skew. Air velocity of 15 – 20 liters per minute is a good starting point. Once the joints have reflowed, the vacuum lift-off should be automatically engaged during the transition from reflow to cool down. Because of their small size the vacuum pressure should be kept below 15 inch of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad liftoff.

### SITE REDRESS

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style soldering iron and desoldering braid. The width of the blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer's recommendations should be followed.

### SOLDER PASTE PRINTING

Because of the small size and fine pitches, solder paste deposition for this package requires extra care. However, a uniform and precise deposition can be achieved if a miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100X magnification. The stencil should then be lowered onto the PCB, and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on the package side also. A

100-micron thick stencil with aperture size and shape same as the package land should be used. Also, no-clean flux must be used, as small standoff of QFN packages does not leave room for effective cleaning.

### COMPONENT PLACEMENT

As the leads are on the underside of the package, a split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. Again, the alignment should be done at 50 to 100X magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

### COMPONENT ATTACHMENT

The reflow profile developed during original attachment or removal should be used to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

## REFERENCES

Please always check Akros website for latest revision of these documents: http://www.AkrosSilicon.com

- Akros Silicon Datasheet: AS1854/34 Datasheet, Rev 1.6, May 2008

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