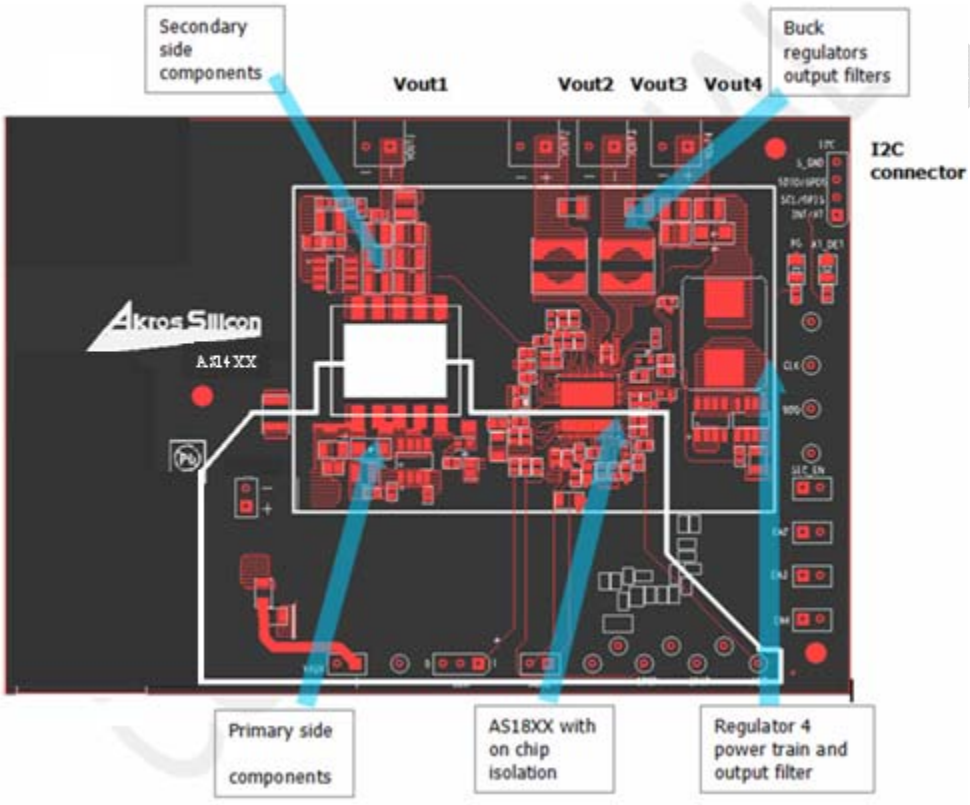
All noise-decoupling capacitors on the AS14x4 traces, such as those connected to SYNC_DLY, VBP, VDD3V_OUT, VDD_SYNC and VDD5I, should be located as close as possible to the AS14x4 and on the same layer as the chip. Placing decoupling capacitors on the bottom layer, below the AS14x4, is not as effective, because the associated high-frequency currents circulate through longer return paths, subjecting the bypassing to higher parasitic inductance.

The VP node (input to the buck regulators), in particular, needs to be bypassed carefully by placing the associated ceramic decoupling capacitors as close to the chip pins as possible.

Figure 28 shows an example layout based on Akros' evaluation board design:

Figure 27 - Component Placement Guidelines



PRIMARY / SECONDARY PCB ISOLATION

The DC-DC converter creates isolated voltages away from the high-voltage signals delivered on the input power lines. Because of this, two independent ground-plane systems must be designed onto the board, one for the high-voltage input side (Primary) and the other for the low-voltage output side (Secondary). This voltage and ground isolation applies to all board layers and components. No traces, pads or vias should be allowed in the isolation gap between the two planes (shown as a solid white line in Figure 28).

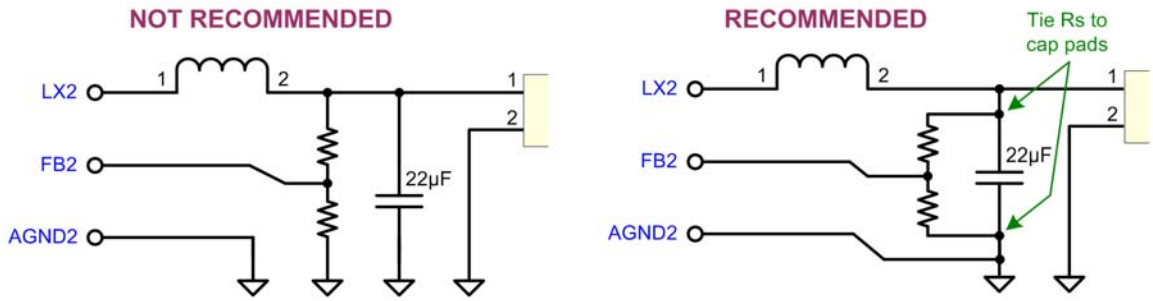
At the beginning of the layout process, designers should plan for the minimum 50mil PCB isolation gap between the Primary and Secondary ground planes. For improved EM performance, it is advisable that the Primary GND be completely encircled by the Secondary GND, as shown in the split white line in Figure . It is recommended, moreover, to clear all copper on all layers from under the transformer.

Note: Designing with the AS14x4 does not require the use of opto-couplers to pass signals across the isolation gap, since the Akros AS14x4 Digital Edge TM Isolation technology already provides clean, digital signal communication between the primary and secondary sides.

SENSE LINES AND FEEDBACK DIVIDERS

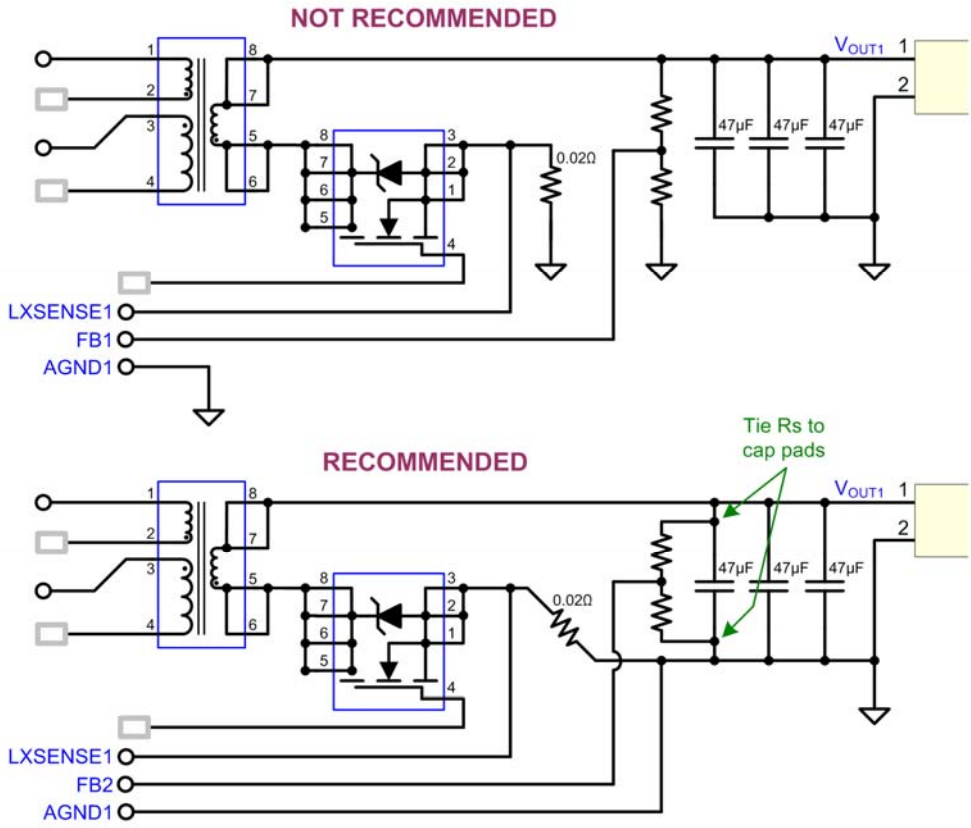
For Outputs 2, 3 and 4, it is important to note that nodes such as AGND2, 3 and 4 may appear on schematics as GND nets, when in fact they belong to their respective feedback-sense grounds, Do NOT connect these pins directly to their associated ground plane by using a via, as shown of the left side of Figure 29. Instead, connect all feedback resistor dividers directly to the output capacitor pads, rather than to the GND planes (as shown on the right side of Figure 29). Route the sense lines (FB2/AGND2) as a differential pair, in parallel and close proximity to each other. The ground planes can be employed as a shield for these and other sensitive signals, to protect them from capacitive or magnetic coupling of high-frequency noise.

Figure 28 - Sense Line Design Practices



For Flyback Output 1, the same sense-line routing practices should be applied as described above for Outputs 2, 3 and 4. Since Output 1 requires an extra sense line (to measure secondary current), it is recommended that the three sense lines be run as shown in Figure 30, for optimum performance.

Figure 29 - Feedback Divider Design Practices



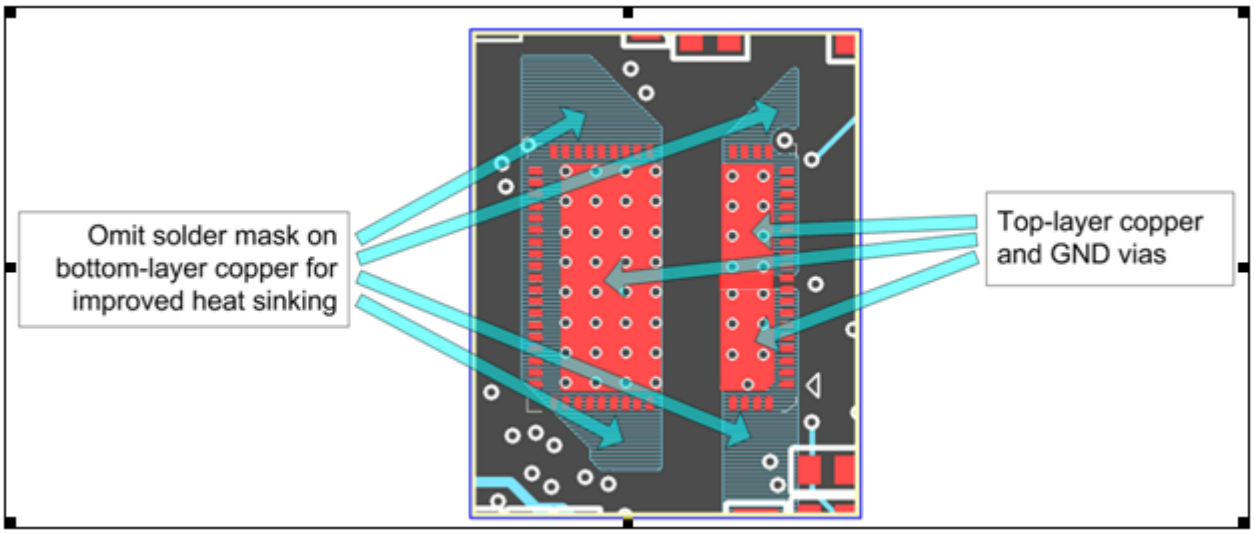
AS14X4 FOOTPRINT

The quad flat no-lead (QFN) package of the AS14x4 provides the advantages of near chip scale package size with very efficient thermal performance. By using the die attach pad of the package as the primary ground path and the direct path of thermal conduction and soldering the entire pad directly to the printed circuit board (PCB), the electrical and thermal resistance of the package to the PCB is drastically reduced. Care must be taken to ensure the thermal path at the PCB interface can properly distribute the heat from the package into the bulk of the board.

Other considerations in the PCB design and assembly in regard to these packages involve PCB finish, pad design, solder mask coverage, via types, solder paste coverage of the signal pads and thermal pads, stencil design, solder joint quality, thermal profiling, and solder past type. Please refer also to "AN083: AX18x4 Assembly Guide" for more details on Akros' recommended best-practices for board-level PCB assembly of the AS14x4 product.

Electrically, the AS14x4 uses pads 1, 2 and 3 on the bottom of the device for electrical connectivity to their associated GND planes. Please make sure to short both the PGND pads on PCB. Thermally, these pads act as heat sinks. Therefore, by adding appropriate numbers of via's connecting each pad to multiple GND planes, excellent thermal and electrical performance can be achieved. Also, it is recommended to add a copper area with no solder mask on the bottom layer, for additional heat dissipation, as shown in Figure 1 below.

Figure 30 - AS14x4 Footprint Design Practices



SUMMARY

Proper electro-magnetic and thermal design practices enhance the performance and reliability of any Switching power supply design. Critical problems regarding layout, trace routing and noise coupling can be avoided with careful pre-layout planning. Designers are encouraged to contact Akros Silicon for guidance on design practices and testing procedures, to minimize or prevent (often hard-to-find) EMI problems in their printed-circuit board architecture.

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