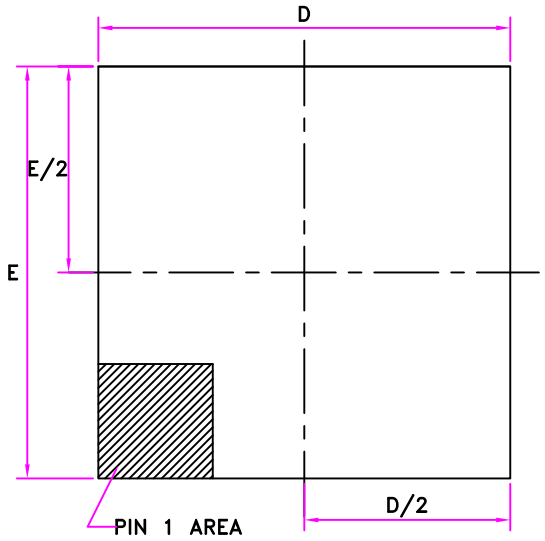
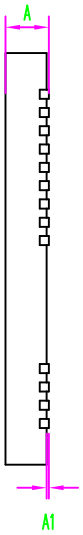
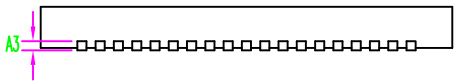
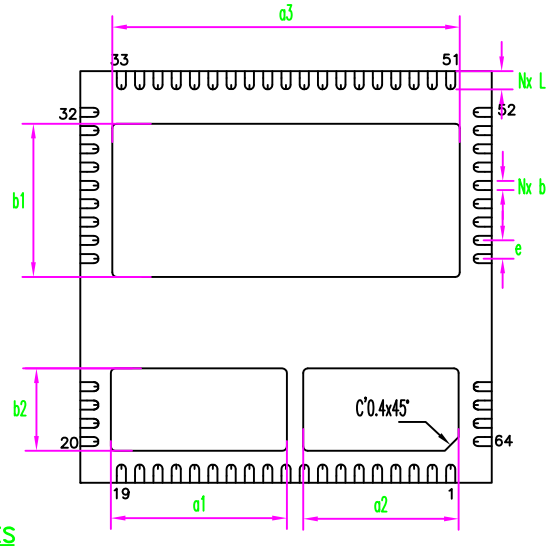
PACKAGE INFORMATION (AS18xx)

PACKAGE: QUAD LEADLESS MOLDED PACKAGE(QLMP)
TYPE:9.0X9.0X0.9 MM (MULTI)









JEDEC#	–N/A–			
TYPE	64 LEAD			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.85	0.95	33.46	37.40
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	8.95	9.05	352.4	356.3
E	8.95	9.05	352.4	356.3
a1	3.8	3.9	149.61	153.54
a2	3.35	3.45	131.89	135.83
a3	7.55	7.65	297.24	301.18
b1	3.3	3.4	129.92	133.86
b2	1.75	1.85	68.90	72.83
e	0.4 BSC		15.75 BSC	
NX b	0.15	0.25	5.91	9.84
NX L	0.35	0.45	13.78	17.72
θ°	0°	4°	0°	4°
ND	19			
NE	13			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.05mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

PREPARED BY	xxx	REF. NO.	REV. NO.	AKROS SILICON
CHECKED BY	xxx	DIM–64L QLMP–9.0X9.0X0.9 (MULTI)	0	USA
APPROVED BY	xxx		DATE 08.02.10	